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GLOBAL PARAMETRIC FAULT IDENTIFICATION IN ANALOG ELECTRONIC CIRCUITS

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Abstract

A method of global parametric fault diagnosis in analog integrated circuits is presented in this paper. The method is based on basic features calculated from a circuit under the test's time domain response to a voltage step, *i.e.* locations of maxima and minima of the circuit-under-test response and its first order derivative. The testing and diagnosis process is executed with the use of an artificial neural network. The neural network is supplied with extracted basic features. After evaluation and discrimination, the output indicates the circuit state. The proposed diagnosis method has been verified with the use of exemplary integrated circuits – an operational amplifier μA741, a sinewave oscillator and an integrated band-pass filter.

Keywords: global parametric fault, identification, artificial neural networks.

1. Introduction

World production of analog integrated circuits increases yearly. Single soft and hard faults, typical for discrete analog circuits, are not the most common ones in analog integrated circuits (AIC) diagnosis [1-5]. The character of integrated circuits manufacturing technology causes a change of faults' profile. Integrated devices of the same type (*e.g.* resistors, capacitors, *etc.*) are usually manufactured in the same process [6-10]. As a result, a critical and proportional change of values of majority (or all) of circuit parameters of one type, beyond their tolerance region, is the major problem. This type of multiple and correlated parametric faults is classified as a global parametric fault (GPF).

Digital circuit testing has been already developed to the point of automation. Yet, analog electronic circuit diagnosis still relies on the test engineers' knowledge and intuition to work out routines allowing for efficient AIC diagnosis [1, 11-14]. The difficulty of analog circuits diagnosis is caused by the complexity of analog signals, a need for anticipation of circuit parameters' tolerances, the complexness of parametric fault models, the influence of a fault propagates toward circuits inputs and outputs, other reasons, too numerous to list.

There are AIC time domain response basic features defined in this paper. Maxima and minima sets, for both circuit response and its first order derivative, are used as a base for the AIC diagnosis. Artificial neural networks (ANN) have been frequently utilized for the purpose of AIC diagnosis (*e.g.* [13, 14]). In this paper, ANN has been utilized for further information processing and GPF location and identification. The presented method requires fault simulation at the before-test stage [1, 15-18].

The method's basic principles have been presented in Section 2. A model of an integrated circuit is demonstrated and employed for the global parametric fault definition.

Basic features, extracted from the circuit under test (CUT) time domain response and its first order derivative are defined.

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Section 3 has been devoted to applications of artificial neural networks for the purpose of global parametric faults identification. ANN outputs are defined with their activation functions (transfer functions). The AIC state is represented by a binary vector. In order to convert the continuous domain into a digital one, discrimination methods are introduced.

The first of the presented methods uses a modified "one hot" circuit states coding and a modified "winner takes all" discrimination strategy. The other two diagnosis routines have employed a natural binary code for the purpose of circuit states encoding

The presented diagnosis methods have been verified, in Section 4, with the use of exemplary circuits – an operational amplifier μA741, a sinewave oscillator and an integrated band-pass filter.

The methods should be utilized at the prototype phase of integrated circuit manufacturing for the purpose of tweaking technological process parameters.

The paper is concluded in Section 5.

2. Basic Principles

2.1. Integrated Circuit and Global Parametric Fault Models

Circuit and global parametric fault models have been constructed with listed assumptions, *i.e*. all circuit parameters of the same type:

- are manufactured in a single process and on a single layer,
- have the same geometrical orientation on a chip, hence photolithographic masks desynchronisation affects them in the same way
- all circuit parameters of one type have the same tolerances [2,6,7].

An analog integrated circuit is defined as a set of grouped circuit parameters:

$$\mathbf{P} = \left\{ P_i^m : i = 1,\ldots,N_m; m = 1,\ldots,M \right\}, \tag{1}$$

where:

- P_i^m – i-th circuit parameter of the m-th group,
- N_m – number of circuit parameters of the m-th group,
- M – number of circuit parameters' groups.

Circuit parameters may be grouped according to their type (*e.g.* resistors, capacitors, diodes, *etc*.), their location on the chip, their orientation on the chip, *etc*. The total number of circuit parameters is given by:

$$E = \sum_{m=1}^{M} N_m \,. \tag{2}$$

A global parametric fault model is essential for the purpose of faulty circuits' performance analysis. The GPF model is given with an equation:

$$\begin{aligned} \mathbf{GPF} = \{ & GPF_j : GPF_j = \delta^m \cdot P_j^m : P_j^m \in \mathbf{P}; \\ & \delta^m \in \langle (1-\alpha_-), (1-\alpha_+ \cdot tol^m) \rangle \cup \langle (1+\beta_- \cdot tol^m), (1-\beta_+) \rangle \}, \end{aligned} \tag{3}$$

where:

- GPF_j – j-th faulty circuit parameter,
- δ^m – the value of circuit parameters deviation,
- tol^m – the tolerance of circuit parameters of the m-th group,
- α_-, α_+, β_-, β_+ – coefficients limiting the possible size of GPF.

GPF (given with an equation (3)) affects all N_m circuit parameters of the m-th group. Circuit parameters' values change δ^m times. Coefficients $\beta_{\pm}$ and $\alpha_{\pm}$ define the maximum and minimum value of the fault. Additionally, α_- and β_+ define the region separating the fault area and the non-faulty area, given with circuit parameters' tolerations.

There has been a gap between areas, in circuit parameters space, defined with circuit parameter tolerances and GPF assumed. In [19], it is proven that it is impossible to determine a faulty circuit under small values of parametric faults. It is caused by a masking effect of a non-faulty circuit parameters.

The aim of testing is determining whether a circuit under test is intact or faulty (GO/NO-GO test). A fault location should answer a question which of the circuit parameters (group of circuit parameters) is faulty. A fault identification provides further information allowing to determine the character and values of faults [1].

The circuit states set is defined by the equation:

$$\mathbf{S} = \{S_s : s = 0,\ldots\theta\}, \tag{4}$$

Taking that each of M circuit parameters group may be faulty:

$$\theta = k_\theta \cdot M, \tag{5}$$

where k_θ=2[1] and the number of all circuit states is θ+1.

Non-faulty and faulty circuits performance may be determined with the use of Monte Carlo analysis. The analysis allows as well to calculate ambiguity areas. If the circuit performance (*e.g.* CUT time domain response features) is within the ambiguity area it is impossible to distinguish circuit states [1].

2.2. Time Domain Response Features

A sampled stimulus is given with a vector:

$$\mathbf{x} = \{x_k : k = 0,\ldots,K-1; x_k = x(t = k \cdot \Delta t)\}, \tag{6}$$

where:

- $x(t)$ – test excitation,
- T_{max} – sampling time
- K – number of samples,
- Δt – sampling step:

$$\Delta t = \frac{T_{\max}}{K-1}. \tag{7}$$

The circuit-under-test response is given with a vector:

$$\mathbf{y} = \{y_k : k = 0,\ldots,K-1; y_k = y(t = k \cdot \Delta t)\}, \tag{8}$$

where $y(t)$ – CUT response, and CUT response first order derivative with a vector:

$$\mathbf{y}' = \{y'_k : k = 0,\ldots,K-1; y'_k = y'(t = k \cdot \Delta t)\}. \tag{9}$$

[1] Broadly, there are two ranges of a parametric fault, *i.e.* "upper", with circuit parameters values greater than the ones given with tolerances, and "lower", with circuit parameters values smaller than the ones given with tolerances.

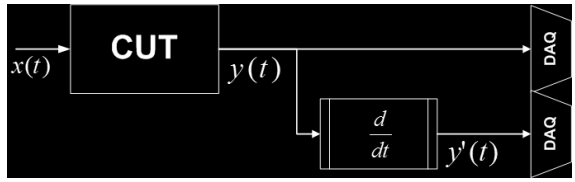

Fig. 1. Testing route.

A testing route is presented in Fig. 1. It has been decided to utilize both circuit's time domain response and its first-order derivative. In case it is impossible to measure (with the use of data acquisition hardware) CUT's response first-order derivative it can be estimated by circuit response's first differential, according to the equation:

$$\mathbf{y}' = \left\{ y'_k : k = 0,\ldots,K-1; y'_k = \frac{y_{k+1} - y_k}{\Delta t}; y_{K-1} = 0 \right\}. \tag{10}$$

Usually, there are several time response features (*e.g.* rise time, steady state value, slew rate and the like) used in analog circuits testing. In the research presented in this paper it has been decided to employ the CUT response and its derivative maxima and minima location. Sets of maxima and minima are given with equations:

$$\begin{aligned} \mathbf{max} = \{ & max_l^d : max_l^d = \left(k \cdot \Delta t, y_k^d\right); \\ & y_k^{(d+1)} = 0; y_k^{(d+2)} < 0; d = 0,\ldots,D-2; l = 1,\ldots L\}, \end{aligned} \tag{11}$$

$$\begin{aligned} \mathbf{min} = \{ & min_l^d : min_l^d = \left(k \cdot \Delta t, y_k^d\right); \\ & y_k^{(d+1)} = 0; y_k^{(d+2)} > 0; d = 0,\ldots,D-2; l = 1,\ldots L\}, \end{aligned} \tag{12}$$

where:

- $D–2$ – the highest order of utilized derivatives (in the presented research $D–2=1$ – first order derivative),
- $D=0$ – denotes the CUT response,
- L – number of analyzed maxima (and minima) locations.

A set of basic features (**BF**) contains the circuit response and its derivative maxima and minima. It is defined as:

$$\mathrm{CB} = \{\max \cup \min\} = \left\{\mathrm{CB}^j : j = 1,\ldots,J\right\}, \tag{13}$$

where:

$$\mathrm{CB}^j = \left\{ CB_i^{j,s} : s = 0,\ldots,\theta; i = 1,\ldots,N_{MC} \right\}, \tag{14}$$

$$CB_i^{j,s} = \left(CB_{x,i}^{j,s}, CB_{y,i}^{j,s}\right), \tag{15}$$

where:

- **CB** – basic features set,
- $\mathbf{CB}^j$ – j-th basic feature,
- J – number of extracted basic features,
- $CB_i^{j,s}$ – i-th sample of j-th basic features for the s-th circuit state[2],
- N_{MC} – number of Monte Carlo analyses run for each of circuit states,

[2] A sample of a basic feature means a random circuit state for which circuit parameter values have been randomly chosen by the means of *e.g.* Monte Carlo analysis.

– $CB_{x,i}^{j,s}$ – x-coordinate of $CB_i^{j,s}$,
– $CB_{y,i}^{j,s}$ – y-coordinate of $CB_i^{j,s}$.

It is possible to present the basic features in rectangular, Cartesian coordinates, whose dimensions, $CB_x^{j,s}$ and $CB_y^{j,s}$, are defined by following basic features. This possibility has been used in the process of GPF identification in [15, 16, 17].

The diagnosis method presented in this paper utilizes artificial neural networks for the purpose of classification of samples of basic features.

3. Artificial Neural Networks

In the presented research an ANN has been used as a CUT response basic features classifier in the process of GPF identification.

The ANN may be described as:

$$\mathbf{ANN} = \{inputs, \mathbf{layers}, outputs\}, \tag{16}$$

where:
– *inputs* – number of the neural network inputs,
– *outputs* – number of the network outputs,

$$\mathbf{layers} = \{layer_a : a = 1, \ldots, A\}, \tag{15}$$

where $layer_a$ – number of neurons in the a-th layer.

The number of ANN inputs depends on the number of basic features. Each basic feature is composed of two numbers (equations (11) – (15)), thus $inputs = 2 \cdot J$. The number of outputs depends on the number of circuit states and the chosen coding.

In the presented work, there have been two coding methods employed:
– a modified "one hot" code,
– a natural binary code.

A bipolar sigmoid transfer function (*tan-sig*) has been implemented in hidden layers' neurons and a unipolar sigmoid (*log-sig*) function in the output layer [20-23].

A training set **trn** contains TR vectors. The corresponding output set is given with **tout**. A validation vector **val** contains VL vectors. In the presented research TF and VL have been chosen in the way that $VL = 3 \cdot TR$. Additionally, $VL + TR = N_{MC} \cdot (\theta + 1)$, where N_{MC} is the number of MC analyses carried out for each of the circuit states.

3.1. Modified "One Hot" Code

Each of ANN outputs is corresponding to one of the circuit states, thus $outputs = \theta + 1$. The main advantage of this coding is the ease of interpretation and finding the natural ambiguity sets.

The ANN output is given with a vector:

$$\mathbf{ANN}^{\mathbf{out}} = \{ANN_{ot}^{out} : ot = 1, \ldots, outputs\}, \tag{16}$$

where ANN_{ot}^{out} is the ot-th ANN output, $\mathbf{ANN}^{\mathbf{out}}$ is a vector of real numbers. It is essential to apply a discrimination procedure. A modified "winner takes all" strategy has been used.

The binary output vector $\mathbf{bANN}^{\mathbf{out}}$ is determined due to the presented procedure:

$$bANN_{ot}^{out} = \begin{cases} 1 & if\ ANN_{ot}^{out,norm} \geq dlvl \\ 0 & otherwise \end{cases}$$

where:

– $dlvl$ – a discrimination level,

– $ANN_{ot}^{out,norm}$ – the ot-th value of $\mathbf{ANN}^{\mathbf{out,norm}}$ vector.

The normalized $\mathbf{ANN}^{\mathbf{out,norm}}$ vector is determined according to the equation:

$$\mathbf{ANN}^{\mathbf{out,norm}} = \frac{\mathbf{ANN}^{\mathbf{out}}}{\max\left(\mathbf{ANN}^{\mathbf{out}}\right)}, \tag{17}$$

If $dlvl<1$ it is possible to determine ambiguity sets. In the presented research $dlvl=0.9$.

3.2. Natural Binary Code

The coding method presented before is characterized by simplicity. A disadvantage of this method of coding is the high number of network outputs. It may lead to a situation in which there are significantly more ANN outputs than inputs or to an unacceptable number of outputs.

A way to limit the number of ANN outputs is to apply a natural binary coding of circuit states. There might be several binary codes chosen, *e.g.* natural, Gray code or error-correcting codes. In this paper there a natural binary code has been utilized.

There have been two implementations of binary coding researched. The difference between methods appears at the ANN outputs' discrimination stage:

– a method employing a fixed discrimination level,

– a method employing a dynamically adjusted discrimination level.

The structure of ANN is the same as in the previously discussed coding method, given by equation (16). The number of outputs is $outputs = \lceil \log_2(\theta+1) \rceil$.

The discrimination in the former of these methods is carried out according to the procedure:

$$bANN_{ot}^{out} = \begin{cases} 0 & if\ ANN_{ot}^{out} \leq (1-mlvl)\cdot dlvl \\ 1 & if\ ANN_{ot}^{out} \geq (1-mlvl)\cdot dlvl \\ 0.5 & otherwise \end{cases}$$

where:

– $mlvl$ – insensitivity level,

– $dlvl$ – discrimination level.

Application of $mlvl \neq 0$ causes a formation of ambiguity sets. In case of a fixed discrimination level $dlvl$ should be the same regardless of the ot-th bit position.

A dynamically adjusted discrimination level may be useful in case of irregular coding, *i.e.* codes that use significantly more *ones* than *zeros* at the ot-th position.

The method of determining the discrimination level can be divided into four stages:

1st stage. For each of the ANN outputs find a sum of bits whose expected values have been either *one* or *zero*:

$$one_{ot} = \sum_{tr=1}^{TR} ANN_{ot,tr}^{out} \wedge tout_{ot} = 1, \tag{18}$$

$$zero_{ot} = \sum_{tr=1}^{TR} ANN_{ot,tr}^{out} \wedge tout_{ot} = 0 . \tag{19}$$

2nd stage. Find the number of ones and zeros for each of the output bits:

$$N_{ot}^{one} = \overline{\overline{\{tout_{tr} : tout_{tr} = 1\}}}, \tag{20}$$

$$N_{ot}^{zero} = \overline{\overline{\{tout_{tr} : tout_{tr} = 0\}}}, \tag{21}$$

where $\overline{\overline{\{(\cdot)\}}}$ denotes a cardinal number.

3rd stage. Calculate average values of zeros and ones for each of the ANN outputs:

$$\overline{one_{ot}} = \frac{one_{ot}}{N_{ot}^{one}}, \tag{22}$$

$$\overline{zero_{ot}} = \frac{zero_{ot}}{N_{ot}^{zero}} . \tag{23}$$

4th stage. Calculate the discrimination level for each of the ANN outputs:

$$dlvl_{ot} = \frac{N_{ot}^{one}}{N_{ot}^{zero} + N_{ot}^{one}} \cdot \overline{one_{ot}} + \frac{N_{ot}^{zero}}{N_{ot}^{zero} + N_{ot}^{one}} \cdot \overline{zero_{ot}} . \tag{24}$$

The discrimination procedure is as follows:

$$bANN_{ot}^{out} = \begin{cases} 0 & if \;\; ANN_{ot}^{out} \le (1 - mlvl) \cdot dlvl_{ot} \\ 1 & if \;\; ANN_{ot}^{out} \ge (1 - mlvl) \cdot dlvl_{ot} \\ 0.5 & otherwise. \end{cases}$$

The existence of "half-bits" has allowed to find ambiguity sets. If there is a "half-bit" in the **bANN^{out}** vector there is the necessity of determining whether all of possible circuit states are correct, *i.e.* if coded circuit states exist[3]. This analysis might allow a simple ANN output correction. Of course, it is possible only if the number of ANN output allows for coding additional circuit states.

4. Examples

The presented diagnosis method has been verified with the use of three computational examples: an operational amplifier μA741 (Fig. 2), a sinewave oscillator (Fig. 3) and an integrated band-pass filter (Fig. 4). All operational amplifiers in the integrated filter have been modelled with the use of a μA741 physical model.

It is necessary to emphasize that there are no documented benchmarks available that would allow for any comparison of methods presented in the paper. For this purpose, two classical classification methods have been applied: a linear classifier and a Nearest Neighbourhood Method classifier. The results of the comparison are discussed in a further part of this paper.

[3] Let's assume **bANN^{out}**=[1{0.5}000], which may code circuit states with ID: 24 or 16. If the number of circuit states θ+1=17 and a natural binary code has been utilized, it is obvious that the only possible solution is circuit states with the ID: 16. A similar analysis shall be applied for all vectors including a higher number of "half-bits".

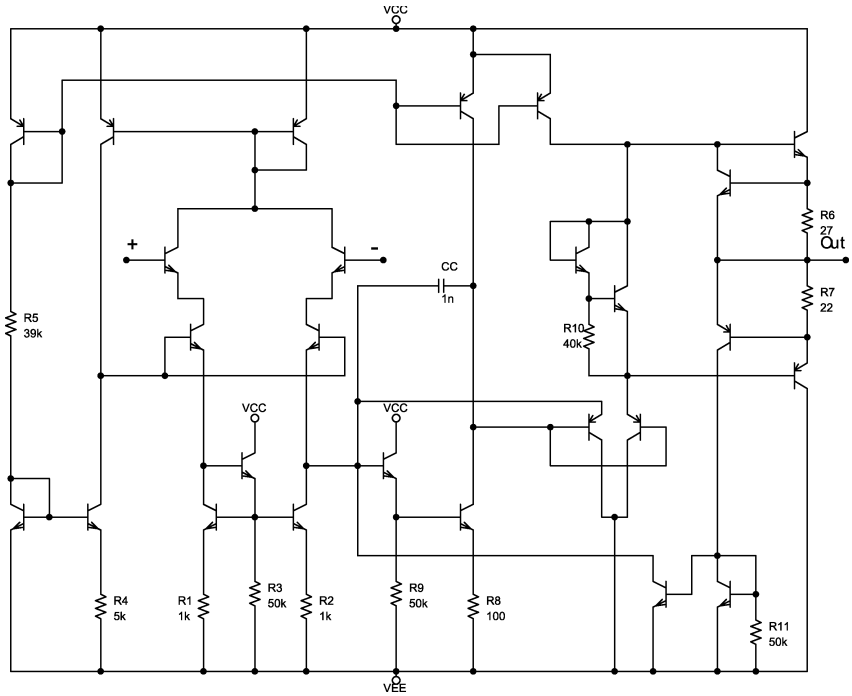

Fig. 2. Exemplary circuit 1 – an operational amplifier μA741.

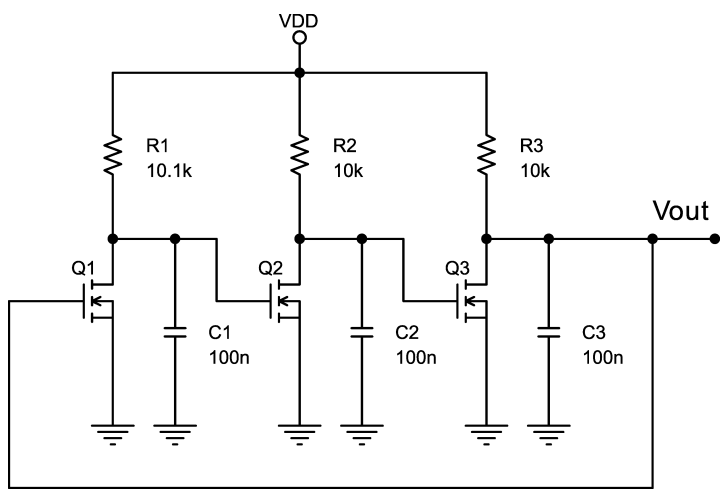

Fig. 3. Exemplary circuit 2 – a sinewave oscillator.

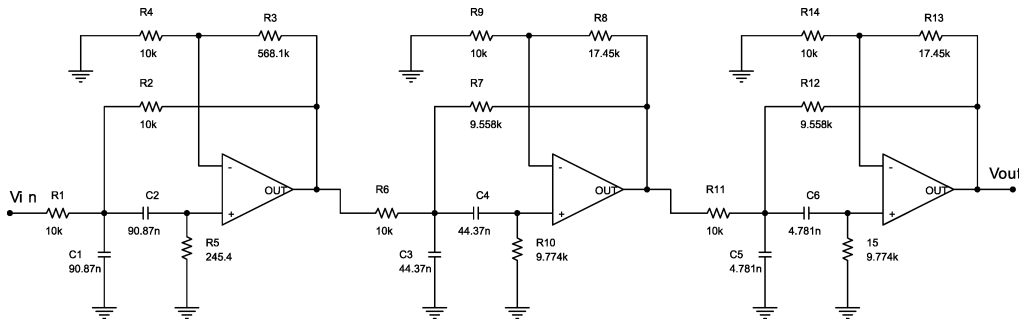

Fig. 4. Exemplary circuit 3 – an integrated filter.

4.1. Diagnosis environment

In this paper, only passive circuit parameters have been considered as possibly faulty. They have been grouped according to their type, *i.e.* resistors and capacitors. It has been assumed that only one circuit parameter group can be affected by a global parametric fault. It has been decided to divide each of the GPF ranges into $\Lambda = 4$ equal sub-ranges, thus the effective number of circuit states has been $\theta = k_\theta \cdot \Lambda \cdot M + 1 = 17$ (k_θ=2 ranges of GPF, Λ=4 sub-ranges, M=2 groups). Introducing sub-ranges increases the resolution of fault identification and thus may carry additional items of information, useful in adjusting manufacturing process parameters

The used GPF model parameters are presented in Table 1. Sub-ranges of GPF for both resistors and capacitors are presented in Table 2 (the presented values are relative). In the notation $X(\sigma \pm \xi)$ X denotes a circuit parameter type (R – resistors, C – capacitors), σ denotes the relative mean value of the fault region ($\sigma = 1$ would mean a nominal value of the circuit parameter) and ξ defines the range of the fault in reference to the relative mean value.

Table 1. Global parametric fault model parameters.

Parameter	Value	Parameter	Value
tol^R	10.0%	tol^C	5.0%
α_-	0.5	α_+	2.0
β_-	2.0	β_+	1.0

Table 2. Global parametric fault sub-ranges.

ID	Circuit state	ID	Circuit state
0	non-faulty		
1	R(0.5375±7.0%)	9	C(0.5500±9.1%)
2	R(0.6125±6.1%)	10	C(0.6500±7.7%)
3	R(0.6875±5.5%)	11	C(0.7500±6.7%)
4	R(0.7625±4.9%)	12	C(0.8500±5.9%)
5	R(1.3000±7.7%)	13	C(1.2125±9.3%)
6	R(1.5000±6.7%)	14	C(1.4375±7.8%)
7	R(1.7000±5.9%)	15	C(1.6625±6.8%)
8	R(1.9000±5.3%)	16	C(1.8875±6.0%)

The margin between the area given by circuit parameter tolerances and the faulty area was equal to $tol^{(\cdot)}$.

A voltage step has been utilized as the test excitation. For each of the circuit states a Monte Carlo analysis of N_{MC}=200 runs has been performed. Both the circuit response and its derivative have been measured.

It has been decided to use a neural network consisting of two hidden layers, $3 \cdot outputs$, for the method with the modified "one hot" coding, and $6 \cdot outputs$, for the method employing a binary code, neurons in each of them.

4.2. Diagnosis results

The diagnosis results are presented in Table 3. For the purpose of a comparison, a circuit states identification with the use of classical classification techniques, *i.e.* a linear classifier and Nearest Neighborhood Method classifier, has been submitted.

Table 3. Diagnosis results.

Circuit	Circuit States Identification Quality Indicator	ANN "one hot"	ANN fixed	ANN adjusted	Linear Class.	NNM Class.
μA741	Detection [%]	92.7	85.3	80.7	80.0	66.0
	False positive [%]	1.1	0.9	0.5	1.6	1.5
	Classified incorrectly [%]	13.5	15.5	15.3	47.4	58.3
	Not classified [%]	0.0	1.7	1.3	0.0	0.0
	Class. unequivocally [%]	84.2	81.5	81.9	52.6	41.7
	Class. 2 elem. ambiguity set[4] [%]	2.3	1.3	1.5	0.0	0.0
	Class. >2 elem. ambiguity set[5] [%]	0.0	0.0	0.0	0.0	0.0
Oscillator	Detection [%]	84.7	78.0	57.3	36.0	35.3
	False positive [%]	1.3	1.5	1.0	8.8	14.2
	Classified incorrectly [%]	16.8	20.7	23.3	63.4	52.7
	Not classified [%]	0.0	2.2	5.4	0.0	0.0
	Class. unequivocally [%]	80.8	74.1	69.4	36.6	47.3
	Class. 2 elem. ambiguity set [%]	2.4	2.9	1.8	0.0	0.0
	Class. >2 elem. ambiguity set [%]	0.0	0.0	0.1	0.0	0.0
Filter	Detection [%]	85.3	70.0	56.3	95.0	10.0
	False positive [%]	0.8	0.5	1.0	0.5	6.0
	Classified incorrectly [%]	16.7	24.9	25.1	49.5	81.5
	Not classified [%]	0.0	1.2	6.8	0.0	0.0
	Class. unequivocally [%]	79.0	72.0	66.0	50.5	18.5
	Class. 2 elem. ambiguity set [%]	3.9	1.8	2.1	0.0	0.0
	Class. >2 elem. ambiguity set [%]	0.4	0.0	0.8	0.0	0.0

All unclassified circuit probes should be interpreted as an *unknown fault* [6]. Ambiguity sets containing a non-faulty state (S_0) have been interpreted as fault-free circuits.

Application of modified "one hot" circuit states coding allowed for acquiring the best results in each of the cases. The detection level has been at least 80.0% which is a satisfactory result. Unequivocal identification remained at the same level (79.0%, the worst result, for the integrated filter).

Reducing the ANN size effected with all identification quality indicators degrading. The most significant changes have been recorded for the method employing a binary code and a

[4] Classified to ambiguity sets consisting of two circuit states. One of them has been classified correctly.
[5] Classified to ambiguity sets consisting of more than two circuit states. One of them has been classified correctly.
[6] A fault that has not been assumed at the faults' simulation state.

dynamically adjusted discrimination level (the unequivocal identification level has dropped below 60%).

Each of ANN applications has led to better results than any classical classification method, regardless of the utilized circuit states coding.

5. Conclusions

A diagnosis of analog integrated circuits is undoubtedly one of the most important issues in nowadays electronic engineering. The character of integrated circuits manufacturing technology influences the fault profile. The most common faults are multiple and proportional parametric faults – global parametric faults.

A circuit states identification procedure has been presented. It is based on basic features classification with the use of an artificial neural network. A set of basic features contains the CUT responses and its first order derivative maxima and minima. The presented approach is characterized by a low signatures dictionary construction cost.

The precision of identification is increased by dividing the global parametric fault range into equal sub-ranges.

The first of the presented methods is based on encoding circuit states with a modified "one hot" binary coding, which allows easy interpretation of identification process results. A method of ANN output discrimination has been presented. It is based on a modified "winner takes all" strategy. The main advantage of this method is a natural ambiguity sets determination. This method requires large neural networks, which may not be acceptable in case of hardware implementations.

This obstacle may be bypassed by coding circuit states with binary codes. This possibility has been utilized in the second and third of the presented diagnosis methods.

The presented diagnosis methods have been verified with the use of three ds computational examples – an operational amplifier (μA741), a sinewave oscillator and an integrated filter. Diagnosis results have been compared with those acquired with the use of two classical classification methods. This comparison has proven that ANN-based methods are more efficient and of a higher quality than classical methods. Limiting the ANN size, by binary coding application, has led to worsening of identification results.

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