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# METHODS FOR ECONOMICAL TEST OF DYNAMIC PARAMETERS ADCS

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**Abstract**

This paper describes two methods for economical test of dynamic parameters ADCs. First method is Exponential Fit Test, second method is Wobbler Test. Common testing methods are mentioned as far the accuracy and time necessary for the complete test are concerned. The tests for fast evaluation of the dependence of an effective number of bits on frequency of input signal are described and the comparison of proposed method with the standard methods is given. The suitable area of proposed method application is "each-piece" factory testing requiring extremely short time testing.

Keywords: ADC Test, Exponentional Fit Test, Wobbler Test, Effective Number of Bits.



## 1. Introduction

There are several common well-described indirect methods of ADC testing that are suitable for an evaluation of the reduction of the Effective Number of Bits (*ENOB*) on the frequency of input signal [1], [2]. For example, the if one has 16-bits AD converter, it is necessary requires to take 64 kilo samples for 0,1 LSB error of estimation of *ENOB* with Sine Wave Fit Test and equivalent number of samples for 0.1dB error of estimation of Signal Noise and Distortion SINAD with Discrete Fourier Transform Test. These series of samples must be taken for each frequency point individually. Similarly to the previous case, the series of harmonic signals must be sampled. It is necessary to avoid leakage error by using coherent sampling.

## 2. Principles of the exponentional fit test

The Exponentional Fit Test is based on best fitting of an exponential signal to the tested digitizer output signal. If samples are acquired from one period of the output signal, it is possible to reconstruct the exponential signal by means of the least-square

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$$x_n = Ae^{-Bt} + C, \tag{1}$$

where $A$ is the reconstructed signal amplitude, $1B$ is its time constant and $C$ is its DC value. The $RMS$ error of this fit $\varepsilon$ denotes the tested digitizer Average Effective Number of Bits is defined

$$\overline{\overline{ENOB}} = n - \log_2\left(\frac{\varepsilon}{RMS_q}\right), \tag{2}$$

where $n$ is the nominal number of digitizer bits and $RMS_q = 2^{-n}/\sqrt{12}$ is the RMS value of its quantizing error.

The exponentional signal is easily generated out of a rectangular signal by means of passive $RC$ element filtration, where the time constant $\tau = RC$, see Fig.1.
The exponentional signal is defined as

$$u_C(t) = U_m\left(1 - e^{-\frac{t}{\tau}}\right), \tag{3}$$

where $U_m$ is the amplitude of the input rectangular signal.

To achieve the final output steady-state signal differing from the theoretical value less than the resolution of the tested digitizer with nominally $n$ bits, the minimum ratio between $T_1$ ($T_2$) and time constant $\tau$ is given by

$$T_{1(2)} \geq \tau\,(n+1)\,ln2 \tag{4}$$

For example, a 16-bit digitizer requires a period of input rectangle $T \geq 11\tau$.

If the duty factor is $T_1 = T_2 = T$ the frequency spectra of both exponential curves are identical and given by the expression

$$A(\omega) = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\tau}\right)^2}} \tag{5}$$

For $\omega >> \tau A(\omega) = \tau/\omega$ and amplitude decreases with a slope – 20 dB/decade, (see Fig. 2.)

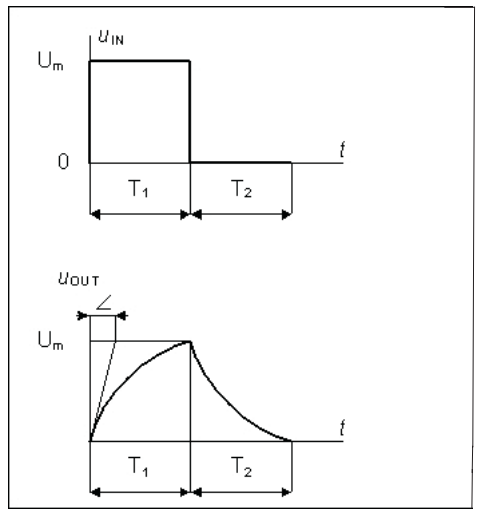


Fig. 1. Exponential signal generation.

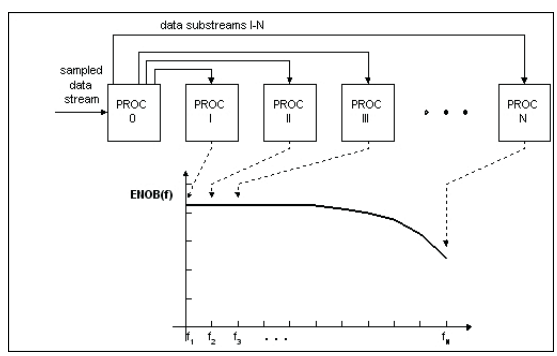


Fig. 2. Frequency spectra of exponentional signal.

## 3. Principles of the wobbler test

The basic idea is to apply the full-scale wobbler signal to the input of the tested ADC located on the chip of the microprocessor. The frequency sweep of the wobbler signal should cover the desired range of dynamic test and the length of the wobbler depends on available memory space for the output series of samples as well as on desired accuracy of the test and on the availability of synchronisation of signal sampling. An estimation of the reduction of *ENOB* due to an increase of the input signal frequency is calculated from measured series of samples. The Fig. 3 shows signal generated in an ADC test.

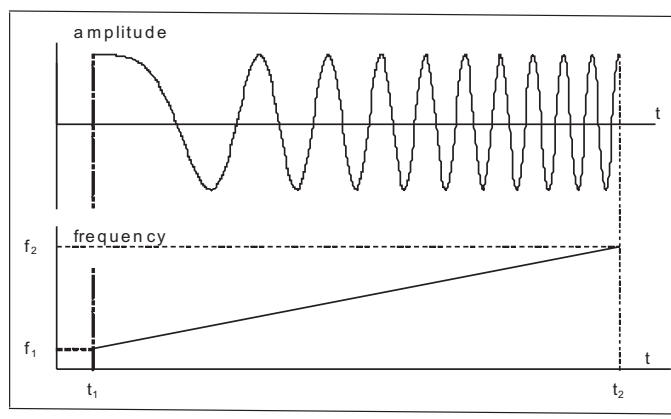


Fig. 3. Wobbler signals generated in ADC test.

The sampling process and the process of chirp generation are controlled by microprocessors. In this case, only one chirp is generated and sampled. The advantage is the reduction of acquisition time (to 50%) but a more complicated arrangement and software are required.

## 4. Algorithm of data processing in the wobbler test

The first step of the algorithm is a rough analysis of sampled data. The measured data stream is divided into substreams. Each substream contains an integer number (one or more to reach the necessary number of samples for the next steps of the algorithm) of quasi-periods of the sampled chir*RMS* calculation). The behavior of the analog input part of the ADC is estimated during this step. The input chirp can be described by the following formula

$$u(t) = A.\sin\left[2\pi\, t\left(\frac{t - t_0}{\Delta t}\,(f_1 - f_2) + f_2\right) + \varphi\right], \tag{6}$$

where $A$ is the amplitude of the chirp, $t_0$ is the start time of the chirp, $\Delta t$ is the duration of the chirp, $f_0$ is the start frequency of the chirp, $f_1$ is the stop frequency and $\varphi$ is the start phase of the chirp. In (1), a linear frequency sweep is considered.

$$\frac{df}{dt} = \frac{f_1 - f_2}{\Delta t}. \tag{7}$$

The least squares algorithm is applied to each substream to fit the ideal quasi period (1) described above to the measured one.To reduce the necessary time of solving the non-linear system equation, not every parameter is optimized during the fitting. In the concrete case $f_0$, $f_1$ are the optimized parameters while other parameters are found by other ways before. Parameter $t_0$ (start time of quasi-period defined as the zero crossing of the measured signal) is calculated using linear interpolation from the two nearest samples (one negative and one positive) samples. In the case of a noisy signal, more complicated higher-order interpolation using more samples should be used. Parameter $\varphi$ is automatically equal to zero when the above described definition of $t_0$ is considered.

Parameter $\Delta t$ (the duration of the current quasi-periods of the chirp) is calculated as the difference of the current t0 and the value of $t_0$ of the next substream.
The effective value of the current quasiperiod – $A$ – is calculated using the following formula:

$$A_{est} = \sqrt{\frac{2}{\Delta t} \sum_{t_i} u^2(t_i)}, \tag{8}$$

where $i$ includes all indices of samples taken between $t_0$ and $t_0 + \Delta t$.

The last step of the algorithm is the calculation of the reduction of *ENOB* on the instant frequency of the input wobbler. The calculation of the Average Effective Number of Bits is done using formula

$$\overline{\overline{ENOB}} = \log_2 \frac{FS}{\sigma_f \sqrt{12}} \tag{9}$$

where $\sigma_f$ is the standard deviation obtained as a final result of chirp fitting of the substream in which

$$f = (f_1 + f_2)/2 \tag{10}$$

Minimum of $\sigma_f$ is the criterion of the best fitting by the least square method.

## 5. Accuracy and speed

The accuracy of the proposed method can be estimated by comparison with the values of sine-fit test for he 16-bit AD converter. The 256 samples must be taken to achieve 0,1 bit accuracy in t estimation of *ENOB*. If each substream contains more

than 256 samples, one can say that the accuracy is equal or better than 0.1 bit (each substream is considered as part of a harmonic signal with the frequency $(f_1 + f_0)/2$). If 20 measured points are necessary to plot the graph showing the dependence of *ENOB* on the frequency, at least 5120 (=20×256) samples must be taken for such accuracy.

A superior chirp generator is required. Most of DDS-based generators are not suitable because the frequency sweep is synthesised from discrete frequency steps and these degrade the results of test.

The proposed test seems to be the fastest way of *ENOB* estimation. The speed of processing may be even enhanced by introducing the multiprocessor approach, see Fig 4.

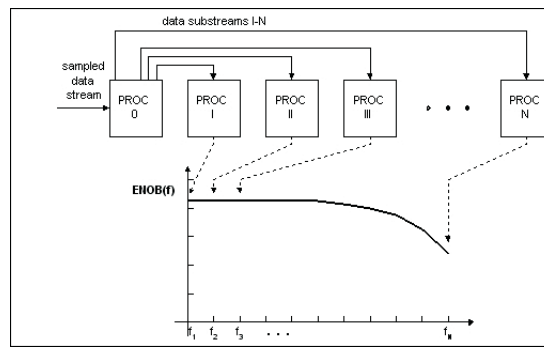


Fig. 4. Multiprocessor approach to test algorithm.

## 6. Comparison and results

Each method described here has been implemented in the internal ADC of the FPGA Start Development Kit Cyclone II by Altera. The internal controlled DDS generator with 24-bit DAC has been used to generate the wobbler signal in a frequency range from 20 Hz to 20 kHz.

The average *ENOB* = 13,9 bits by Exponential Fit Test and average *ENOB* = 14,1 bits by Wobbler Test in the frequency range up 20 Hz to 20 kHz is relevant to *ENOB* plot, determined by the classical Sine Wave Fit Test method. In Fig. 5 is presents the *ENOB* plot for internal ADC by Sine Wave Fit Test. The average *ENOB* by this method is 14,2. The difference of 0.3 bit between *ENOB* and $ENOB_M$ is practically insignificant.

In Fig. 6, Fig. 7 and Fig. 8 the FFT plot of Noise Histogram Test with grounded input, Code Words Histogram Test and FFT plot of sinus signal 1 kHz are presented. The Effective Resolution of internal converters under test defined by formula

$$ER = \log_2 \frac{FS}{RMS_{NOISE}} \tag{11}$$

is 15,4 bits. In the FFT plot in Fig.6, evident parasitic spectral components with USB supply noise under 100 dB are evident.

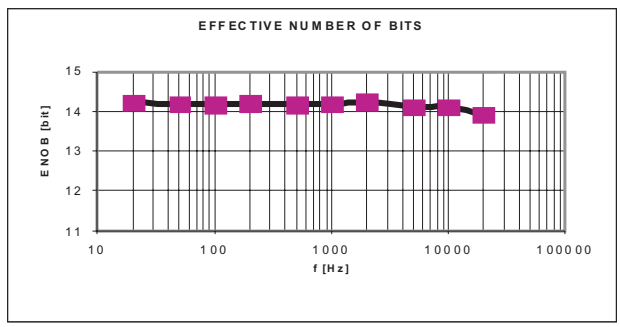


Fig. 5. ENOB plot for Sin Wave Fit Test by FPGA from Altera.

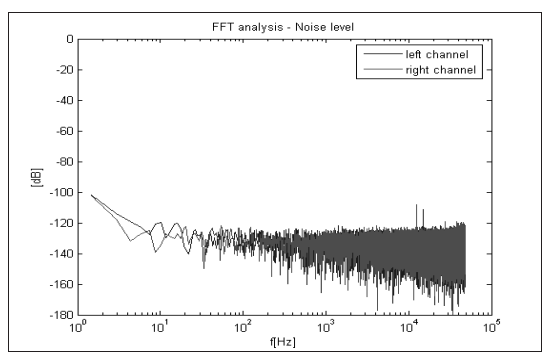


Fig. 6. FFT plot of Noise Histogram Test.

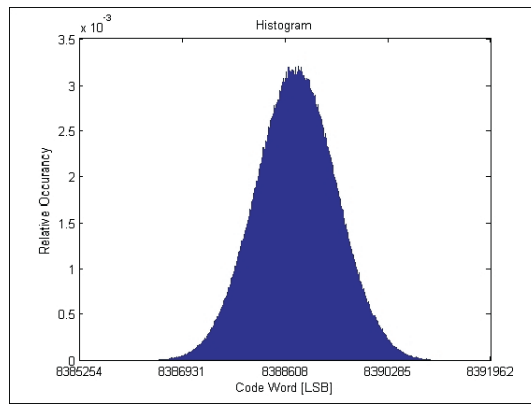


Fig. 7. Code words histogram test.

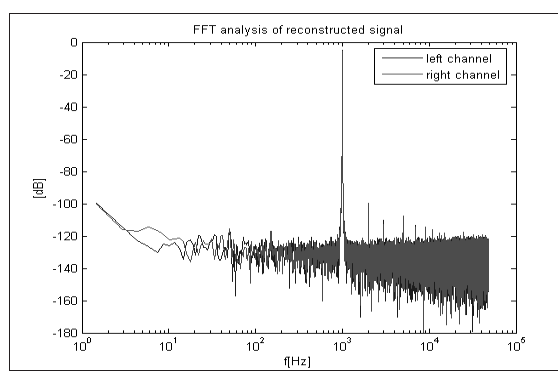


Fig. 8. FFT plot of sinus signal 1 kHz.

In Table 1 is a comparison of results of all tests applied to the internal ADC in FPGA Altera II.

Other parameters in Table 1 are: THD (Total Harmonic Distortion), SFDR (Spurious Free Dynamic Range) and SNHR (Signal to Non-Harmonic Ratio).

From measured examples in Table 1 a very large reduction of the number of samples in application of the Wobbler Test and Exponentionel Fit Test is evident. The reduction of samples is very significant for economical aspects of dynamic testing of internal ADC in embedded Data Acquisition Systems.

Table 1. Comparison results of ADC test.

| Sine Wave Fit Test and Discrete Fourier Transform Test | | | Wobbler Test | Exponential Test |
|---|---|---|---|---|
| Frequency of input signal | 1 kHz | 10 kHz | 20Hz – 20kHz | |
| *ENOB* | 14,7 bit | 13,8 bit | 14,1 dB | 13,9 dB |
| *SINAD* | 90,2 dB | 84,8 dB | | |
| *THD* | 103 dB | 95 dB | | |
| *SFDR* | 102 dB | 92 dB | | |
| *SNHR* | 94 dB | 86 dB | | |
| *ER* | 15,4 bit | | | |
| Number of samples | 64 k In 10 steps of frequency range 20Hz – 20kHz | | 5120 | 1024 |

## 7. Conclusions

In the article is two high-speed test methods are proposed. Due to the high speed of the test, the method described above can be suitable when the necessity of testing of many pieces of ADC is required, *e.g.* at the end of a manufacturing process.

## Acknowledgements

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