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PARTICULARITIES OF THE CYCLIC A/D CONVERTERS ENOB DEFINITION AND MEASUREMENT[1],[2]

The paper is devoted to the methods of accurate assessment and analysis of the expected and actual effective number of bits (ENOB) of cyclic analog-to-digital converters. The equivalence of definition of ENOB in the IEEE Standard 1241-2000 and proposed in earlier author's works analytical definition formulated on the basis of distributions of the input signal and conversion errors. Indirect and direct methods of ENOB measurement are considered. The presented results can be used for a development of accurate methods of performance analysis and testing of the cyclic and other ADCs.

Keywords – analog-digital conversion, cyclic, intelligent ADC, ENOB, converter's performance

1. INTRODUCTION

High requirements to the speed and accuracy of conversion under general tendency to diminish the sizes, cost and power consumption of analog-to-digital converters (ADC) converters are best satisfied in the cyclic converters (CADC). The main factor complicating the development of theoretical support of the design of both ADC and CADC is multiple non-linearity of the ADC's transition function conditioned by the finite input range of the converters, non-linear mapping of the continuous set of analogue input signals into the discrete set of output codes, and by non-uniform setting of quantization thresholds. These non-linearities create significant difficulties in formulation of adequate characteristics of the conversion quality [1-4] and, as a consequence, in the development of mathematically grounded methods of their measurement. A not less important and unsolved task is an optimization of the architecture and parameters of CADC enabling full utilization of the resources of their analogue and digital components improving the converter's performance. These circumstances complicate the design

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[2] The work was presented at *IEEE Instrumentation and Measurement Technology Conference (IMTC 2006)* [5]

of the converters and worsen their actual characteristics in comparison with those potentially achievable.

Nowadays, most commonly used measures of ADC performance are the effective number of bits (ENOB) and an equivalent measure – effective resolution (EFR) [1, 3–5], signal-to-noise and distortion ratio (SINAD), total harmonic distortion (THD), differential (DNL) and integral (INL) nonlinearities, and some others [1, 2]. Except of ENOB, all the listed measures of conversion quality are determined for pure sine-wave testing signals with specified amplitude and frequency. However, non-linearity of the ADC violates the principle of superposition; that makes the results of sine-wave tests approximate and sensitive to the changes of the form and parameters of the sinusoid. This decreases the reliability of the test results and radically increases the requirements to the form and parameters of the harmonic testing signals. Another disadvantage of sine-wave tests is non-uniformly weighed numerical assessment of quantization thresholds ("code transition levels" [1]) setting errors. The latter effect is caused by the slow changes of the signal near its extremes, specific for the harmonic signals, and fast changes near the zero values. As the result, the accuracy of quantization threshold measurements decreases in the central and increases in the upper and bottom regions of the ADC input range. At last, the sine wave cannot be considered as a typical signal at the ADC input. For these reasons, the search for more accurate characteristics of conversion quality, independent of the testing signals, as well as for accurate and methods of their measurement, convenient for applications, remains an unsolved issue in ADC design [2, 3].

Recently, researches in this direction are focused on measurements of the *flash* ADC performance. Other classes of converters, such as the cyclic ADC (sub-ranging, successive approximation, $\Sigma\Delta$, redundant sign digit, others) and pipe-line (cascade) ADC, are measured as "black boxes" and analysed using the methods and measures of quality used in the flash ADCs analysis and testing. However, investigations [5–10] and other show that these methods and measures cannot be directly applied to the analysis of cyclic ADC (CADC) and pipe-line ADC (PADC) and should be corrected. The necessity of corrections follows from the established fast normalization of quantization errors for the greater number of cycles or cascades of conversion [6, 7]. This violates the commonly used assumption, valid for high-quality flash ADC, that the conversion errors are distributed uniformly inside of each quantization interval. As the result, all the characteristics of CADC and PADC using this assumption also become inadequate.

An additional difficulty following from the "black-box" approach to CADC and PADC analysis is the impossibility to determine the dependence of the conversion quality on the architecture, parameters and non-idealities of the analogue part, internal noise and distortions. For the same reason, definition of integral and differential non-linearities of CADC and PADC loses its sense. Also, a "black-box" approach does not permit to investigate the processes inside the converters, including the changes of accuracy and reliability of codes formed in sequential cycles or stages of conversion.

The paper generalizes the results of work [5] devoted to development of accurate formal methods of ADC performance analysis, optimization and testing. The investigation is performed for the case of the *cyclic* ADC. Special attention is paid to necessary correction of known

definition of ENOB and to the principles of ENOB measurement. There are considered indirect and direct methods of ENOB measurement initially studied in [6, 7]. Analysis of the direct method shows its advantage over conventional indirect methods of ENOB assessment [3, 4] due to exclusion of intermediate operation – estimation of the root mean square (*rms*) error of conversion. Direct measurement of ENOB permits also to apply optimal estimation theory and compute its estimates using extended optimal adaptive algorithms [11, 12]. Although the analysis is carried out for cyclic ADC, the presented analytical tools and qualitative results of investigation can be applied to the analysis and design of other classes of CADC, PADC and, in part, of the flash ADC.

2. MATHEMATICAL TOOLS FOR ANALYSIS OF CYCLIC CONVERTERS

The approach and mathematical tools presented in [6-10] can be applied to the analysis of both conventional and intelligent cyclic ADC (IC ADC). The term "intelligent CADC" reflects their particularity of functioning: both forming of the output codes and adaptation of the analogue part are performed on the basis of permanently corrected model of the input excitation and predictions of its evolution [13]. To explain the principles of intelligent conversion and the sources of its advantages over known methods of cyclic conversion, below we compare the architectures of IC ADC and CADC (see Figs. 1, 2), methods of forming the input signal codes and mathematical models of both classes of the converters. As a specimen of CADC, the known sub-ranging converter ADI-1678 [13] is considered. The architecture and functioning of IC ADC are considered on the level of generalization adopted in [6-10].

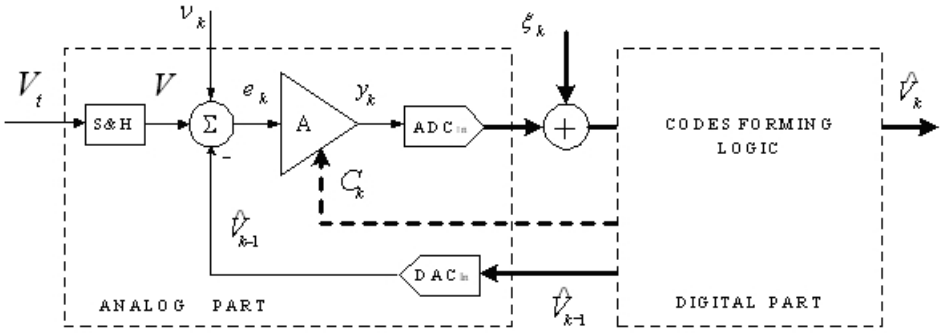

Fig. 1. General structure of CADC.

Comparison of the converters shows that their analogue parts have identical architecture and differ only in the gains of amplifiers (A). Digital parts of the converters differ both in construction and method of final codes forming.

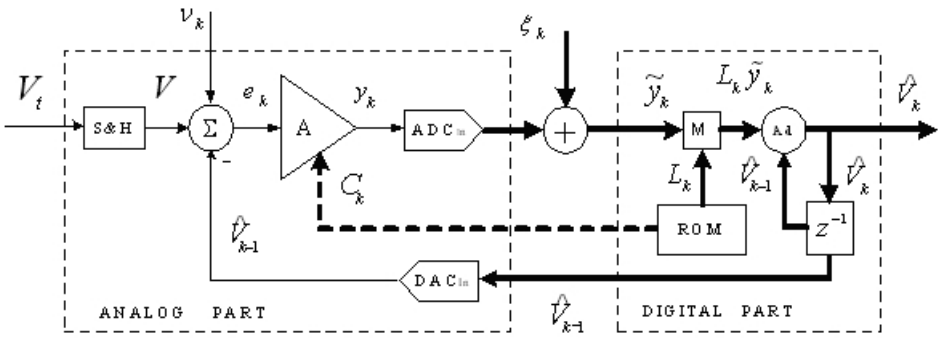

Fig. 2. General structure of intelligent CADC.

2.1. Main mathematical models

To enable a formal description of the conversion process, mathematical models of the input signals, analogue and digital parts of the converters should be given. We assume that the input signals $V_t = V(t)$ are zero mean Gaussian random processes with the power not greater than the given value σ_0^2 and spectral power density equal to zero outside the frequency band $[-F, F]$. The sample-and-hold block (S&H in Figs. 1, 2) holds the value of the sample $V^{(m)} = V(m/2F)$, $m = 1, 2, \ldots, M$, at the first input of subtracting block Σ during the interval $T = 1/2F$. Each sample $V^{(m)} = V(m/2F)$ of the input signal is converted in the same way, in $n = F_0/2F$ cycles, independently of the results of conversion of the previous sample (F_0 is the pass-band of the analogue part of the converter). This permits to reduce the analysis of CADC work to consideration of the conversion of a single sample $V^{(m)} = V$ which, in turn, permits to reduce the model of the input signal to the form of a sequence of adjacent rectangular pulses with normally distributed amplitudes, sufficient for initial research.

In each cycle, the intermediate code $\hat{V}_k$ of the sample V is formed using previous code $\hat{V}_{k-1}$ and digital "observation" – code $\tilde{y}_k$ formed by the N_{ADC} – bit coarse pre-converter $\mathrm{ADC_{In}}$ at the output of the analogue part ($N_{ADC} = 1 \div 6$bits, depending on the type of CADC). This process can be described by the recursive equation common for all CADC:

$$\hat{V}_k = \hat{V}_{k-1} + L_k \tilde{y}_k; \ (k = 1,...,n), \tag{1}$$

which can be treated as a mathematical (input-output) model of the processes in the digital part of the CADC. Values of the gains L_k in (1) depend on the type of CADC. Mathematical model of the analogue part describing transformation of the input sample V into observations $\tilde{y}_k$ can be introduced in the form of a piece-wise linear static transition function [6-12] applicable for the analysis of each CADC:

$$\tilde{y}_k = \begin{cases} C_k e_k + \xi_k & \text{for } C_k |e_k| \le D; \\ D sign(e_k) + \xi_k & \text{for } C_k |e_k| > D, \end{cases} \tag{2}$$

where $e_k = V - \hat{V}_{k-1} + v_k$ are the residual signals formed by the subtracting block Σ and routed to the input of amplifier A. Value $\hat{V}_{k-1}$ represents here the analogue equivalent of one-step prediction of the sample value: $\hat{V}_{k,k-1} = E(V \mid \tilde{y}_1^{k-1}) = \hat{V}_{k-1}$ formed by the digital part of CADC in the previous cycle. Noise v_k is the sum of the noise of the feedback chain, S&H block, subtractor Σ and possible external noise. In the present work, noise v_k is considered as zero-mean white Gaussian noise with the variance σ_0^2. Parameter D determines the boundaries $[-D, D]$ of the full scale range (FSR) of pre-converter ADC_{In}. Noise ξ_k is the quantization noise at the ADC_{In} output describing the distortions caused by the step-wise form of the transition function. According to the commonly used approach, this noise is assumed to be uniformly distributed inside of the quantization interval $[-\Delta_{ADC}/2; \Delta_{ADC}/2] = [-D/2^{N_{ADC}-1}, D/2^{N_{ADC}-1}]$), and its variance is determined by formula:

$$\sigma_\xi^2 = \frac{\Delta_{ADC}^2}{12} = \frac{D^2}{3} 2^{-2N_{ADC}}. \tag{3}$$

2.2. Constraints on the parameters of conventional CADCs

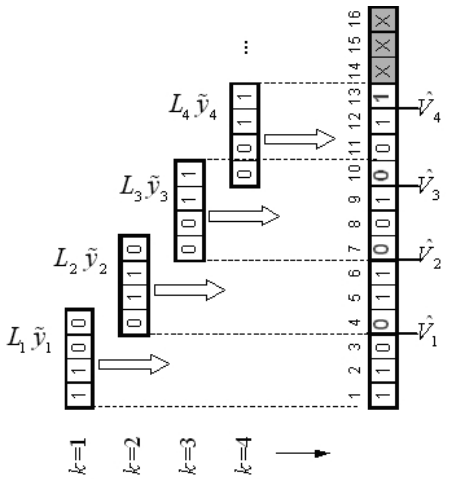

Fig. 3. Codes forming in conventional CADC [14].

Depending on the type of CADC, digital gains L_k in (1) and analog gains C_k in (2) may have fixed or subsequently switched values connected by the reversed dependence: $C_k = L_k^{-1}$. In conventional CADCs, decimal values of the gains L_k are determined by parameters of the shifting elements in the digital part. In each cycle, before being added to the previous code $\hat{V}_{k-1}$,

observations $\tilde{y}_k$ should be shifted up by $N_k = \Sigma_{i=1}^{k-1}(N_{ADC} - m_i)$ positions (see Eq. (1) and Fig. 3). Values m_k represent here the number of least significant bits (LSB) reserved for the correction of possible errors in the intermediate codes $\hat{V}_{k-1}$ usually realized as overlapping of m_k bits of codes $\hat{V}_{k-1}$ and $L_k\tilde{y}_k$ [14]. For this reason, in conventional CADC, the decimal form of the gains L_k and analogue gains C_k always has the form of integer powers of two:

$$C_k = C_1 2^{\Sigma_{i=1}^{k-1}(N_{ADC} - m_i)} = L_k^{-1}. \tag{4}$$

Initial values C_1 and L_1 are determined by the ratio of FSR of pre-converter $\mathrm{ADC_{In}}$ to FSR of CADC, and also must be equal to the integer powers of two. Final resolution of CADC after *n* cycles is equal to $N_{fin} = \Sigma_{i=1}^{n}(N_{ADC} - m_i)$.

2.3. Principles of intelligent A/D conversion

Intelligent and conventional CADC have identical analogue parts and differ in the principle of code forming and in realization of the digital part (see Figs 1, 2). Unlike CADC, in IC ADC each intermediate code $\hat{V}_k$, ($k = 1, \ldots, n$) is actually *computed*, according to the same recursion (1) in the form of N_{comp}-bit binary word, ($N_{comp} = 16$, 24 or 32 bits depending on required final resolution of IC ADC). The digital multiplier M placed at the input of digital part of IC ADC computes, in each cycle, the N_{comp}-bit binary product $L_k\tilde{y}_k$ of N_{comp}-bit gain L_k and N_{ADC}-bit observation $\tilde{y}_k$. The computed code $L_k\tilde{y}_k$ is added in the adder (Ad) to the estimate $\hat{V}_{k-1}$ computed in the previous cycle. New N_{comp}-bit estimate $\hat{V}_k = \hat{V}_{k-1} + L_k\tilde{y}_k$ is routed from the adder to one-cycle storing unit z^{-1} and to the input of feedback D/A converter $\mathrm{DAC_{In}}$. The analog equivalent $\hat{V}_k$ of this estimate is routed to the second input of the subtracting block and a new cycle of conversion begins.

This process is illustrated in Fig. 4 where changes of "true" non-erroneous bits (denoted by zeros) in the codes $\hat{V}_k$, $k = 1, 2, \ldots$ are presented.

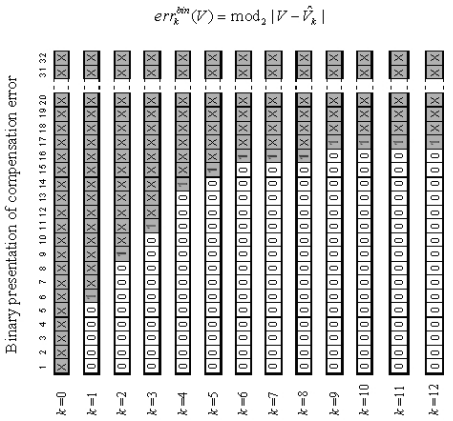

Fig. 4. Codes forming in intelligent CADC.

Transition to the long-word arithmetics in IC ADC removes constraint (4) on the values of gains L_k, C_k and permits to set the analogue gains C_k to the values somewhat greater than in conventional CADC. This increases the signal-to-noise ratio (SNR) at the output of pre-converter $\mathrm{ADC_{In}}$ and improves the quality of estimates. However, gains C_k can be increased only till a definite value, above which the probability of CADC overloading exceeds the given permissible value μ. Optimal values C_k and L_k which minimize MSE of conversion $P_k = E[(V - \hat{V}_k)^2]$ under given μ are determined, for each cycle, by the following formulas [6-10, 12] (values L_k are presented in decimal form):

$$C_k = \frac{D}{\alpha\sqrt{\sigma_v^2 + P_{k-1}}}, \qquad L_k = C_k^{-1}\left(1 - \frac{P_k}{P_{k-1}}\right) \tag{5}$$

and

$$P_k = \left(1 + \frac{C_k^2 P_{k-1}}{\sigma_\xi^2 + C_k^2\sigma_v^2}\right)^{-1} P_{k-1} = (1+Q^2)^{-1}\left(1 + \frac{\sigma_v^2 Q^2}{\sigma_v^2 + P_{k-1}}\right)P_{k-1}, \tag{6}$$

where:

$$Q^2 = SNR_k^{ac} = \frac{C_k^2 E(e_k^2)}{\sigma_\xi^2} = \frac{W_{signal}}{W_{noise}} = \left(\frac{D}{\alpha\sigma_\xi}\right)^2 \tag{7}$$

is the maximal value of SNR at the $\mathrm{ADC_{In}}$ output. Value $W_{signal} = C_k^2 E(e_k^2) = (D/\alpha)^2$ is the power of the useful component of the signal $\tilde{y}_k$; and $W_{noise} = \sigma_\xi^2$ is the power of quantization noise of pre-converter $\mathrm{ADC_{In}}$. The saturation factor α in (5) – (7) is connected with the permissible probability of overloading μ by the relationship:

$$\Phi(\alpha) = \frac{1}{\sqrt{2\pi}}\int_0^\alpha \exp\left(-\frac{x^2}{2}\right)dx = \frac{1-\mu}{2}, \tag{8}$$

where: $\Phi(\alpha)$ – is the Gaussian error function. Probability μ determines the probability $\gamma = 1 - (1-\mu)^n \approx n\mu$ of appearance of distorted codes at the IC ADC output, which coincides with the *word error rate* (WER) introduced in IEEE Standard 1241-2000 ([1], p. 4.13) as an independent characteristic of the conversion performance. Initial values for recursions (1), (6) are determined by the mean value $\hat{V}_0 = 0$ and permissible power $P_0 = \sigma_0^2$ of the input signal, respectively.

One should notice that gains (5) are strictly optimal only if distributions of random values and noise in models (1), (2) are Gaussian [11, 12]. The step-wise form of the $\mathrm{ADC_{In}}$ transition function makes distribution of quantization noise ξ_k non-Gaussian. For this reason, values (5) are only close to the optimal ones (*sub-optimal*) and can be corrected in the way improving the final resolution of IC ADC [8-10].

3. DISCRETE SCALE OF CODES AND ENOB

In works [6, 7] it was established that independently of the form and distribution of the input signal, distribution of final code errors in IC ADC quickly normalizes. In Figure 5, changes of histograms of conversion errors in sequential cycles are shown. Plots in Figs. 5a, b are obtained in simulation experiments as the result of conversion of $M = 10\,000$ samples of a sinusoidal input signal, plots in Fig. 5c correspond to a random, uniformly distributed input signal. The results show that beginning with the "threshold" number of cycles n^*, all histograms take the Gaussian form.

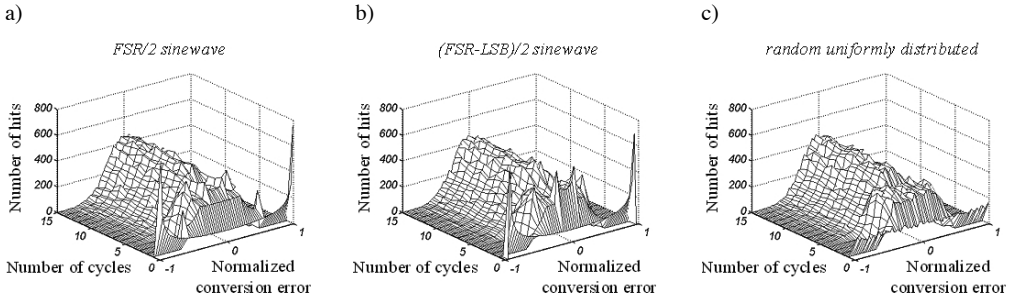

Fig. 5. Evolutions of histograms of conversion errors versus number of cycles under different classes of the input signals: a) FSR/2 sine wave; b) (FSR-LSB)/2 sine wave; c) random uniformly distributed signal.

The threshold number of cycles corresponds to the instant of time when *rms* of conversion errors $\sigma_k = \sqrt{P_k}$ (*rms noise* in terms of [1]) reaches the value σ_v of rms of the analogue noise at the amplifier (A) input: $\sigma_k = \sqrt{P_k} = \sigma_v$. One can show that the threshold value n^* determines the optimal number of conversion cycles and can be assessed according to the formula [6-10, 12]:

$$n^* = \frac{1}{\log\,(1+Q^2)} \log\left(\frac{\sigma_0^2}{\sigma_v^2}\right). \tag{9}$$

The distribution of conversion errors for $k \geq n^*$ takes the form:

$$p(V \mid \tilde{y}_1^k) = p(V \mid \hat{V}_k) = (2\pi P_k)^{-\frac{1}{2}} \exp\left\{-\frac{[V - \hat{V}_k]^2}{2P_k}\right\}. \tag{10}$$

Using (10), one can easily show that values of the signal V, which produce the code word $\hat{V}_k$, lie in the interval $[\hat{V}_k - \Delta_k/2;\ \hat{V}_k + \Delta_k/2]$, $(\Delta_k = 2\alpha\sqrt{P_k})$ with a probability not smaller than $1 - \mu$.

3.1. Discrete scale and ENOB of an ideal IC ADC

Let us divide the FSR $[-V_0^{\max}, V_0^{\max}]$ of an IC ADC into $M_k = FSR/\Delta_k$ adjacent intervals $[V_k^{(i-1)}, V_k^{(i)}] = [-V_0^{\max} + (i-1)\Delta_k ; -V_0^{\max} + i\Delta_k]$ each of the width $\Delta_k = 2\alpha\sqrt{P_k} = 2\alpha\sigma_k$ ($i = 1, \ldots, M_k, k = 1, 2, \ldots$). According to what has been said above (see also Fig. 5), the distance between each analogue value V from the interval $[V_k^{(i-1)}, V_k^{(i)}]$ and its central point $\hat{V}_k^{(i)} = -V_0^{\max} + (i - 1/2)\,\Delta_k$ is not greater than $\Delta_k/2$ with the probability $1-\mu$. This means that each discrete value $\hat{V}_k^{(i)}$ can be considered as the result of measurement of the input sample V with the error practically never greater than $\pm\Delta_k/2$. It is easy to notice that the value $\hat{V}_k^{(i)}$ can be replaced by the number of corresponding interval. In turn, the number of bits necessary for unambiguous binary presentation of the numbers $i = 1, \ldots, M_k$ of intervals $[V_k^{(i-1)}, V_k^{(i)}]$ is equal to:

$$N_k = \log_2 M_k = \log_2\left(\frac{FSR}{2\alpha\sqrt{P_k}}\right) = \log_2\left(\frac{FSR}{2\alpha\sigma_k}\right). \tag{11}$$

On the other hand, each N_k-bit binary word $\hat{V}_k^{(i)}$ determines a corresponding set $\Omega_k(\hat{V}_k^{(i)})$ of possible values of the computed N_{comp}-bit estimates $\hat{V}_k$, ($N_{comp} > N_k$) which begin with identical sequence of N_k most significant bits $\hat{V}_k^{(i)}$. It is easy to see, that each "continuous" N_{comp}-bit estimate $\hat{V}_k$ from the set $\Omega_k(\hat{V}_k)$ can be replaced by the discrete estimate $\hat{V}_k^{(i)}$, which consists of N_k initial bits of the code $\hat{V}_k$, and $\hat{V}_k^{(i)}$ is the code of the input sample V measured with an error not greater than $\pm\Delta_k/2$. The latter shows the way of accurate transition from continuous to discrete scale of estimates with the scale unit Δ_k. Formula (11) determines the mean number of significant bits in the computed estimates $\hat{V}_k$ which has the same sense as the effective number of bits (ENOB) introduced in [1]. One should notice that formula (11) is valid in the case of normal distribution of quantization errors and ideal (equidistant quantization levels) transition function of the analogue part of IC ADC.

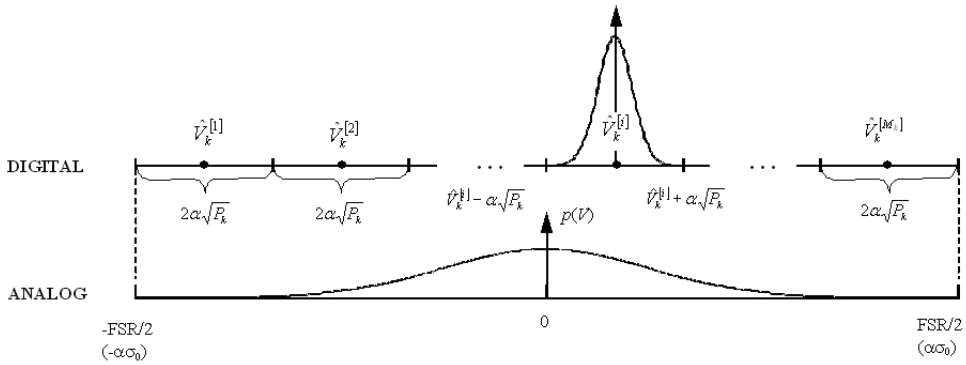

Fig. 6. Illustration of transition to discrete scale of estimates.

For Gaussian input signals, FSR of the converters can be determined as the interval $[-V_0^{\max}, V_0^{\max}] = [-\alpha\sigma_0, \alpha\sigma_0]$ where $\sigma_0^2 = P_0$ is the maximal permissible power of the input signals

(choice α = 3 refers to "three sigma" FSR. Nowadays, values α = 4 and 5 are usually taken. For the threshold mode of conversion (conversion of each sample is finished after a *threshold number* of cycles $n = n^*$ and $\sigma_n = \sqrt{P_n} = \sigma_v$), taking into account FSR = $2\alpha\sigma_0$, formula (11) for ENOB of an ideal IC ADC can be rewritten in the form:

$$N_{n^*} = N^* = \log_2\left(\frac{\sigma_0}{\sqrt{P_n}}\right) = \frac{1}{2}\log_2\left(\frac{\sigma_0^2}{P_n}\right) = \log_2\left(\frac{\sigma_0}{\sigma_v}\right). \tag{12}$$

Left terms of this formula are accurate for $n \geq n^*$ cycles of conversion. For $n < n^*$, this term can be used for approximate evaluation of ENOB of an ideal IC ADC [5-10].

It is necessary to remember that formula (11) is valid only if overloading of the converter is excluded with a probability not less than 1- μ. For conventional, non-optimal CADC this probability, as well as the word error rate (WER), is not a characteristic of special importance and, apart from the case high-precision converters, can be omitted. However, in each sub-optimal ADC where close to full utilization of resources of the analogue and digital elements is achieved, ENOB and WER are mutually connected and WER becomes a not less important characteristic of conversion quality. In practical applications, WER can be replaced by the equivalent characteristic – *bit error rate* (BER) widely used in digital communications [15].

3.2. Relation between standard and introduced ENOB definitions

The definition of ENOB given in IEEE Standard 1241-2000 ([1], p. 4.5.2) for flash ADC has the form

$$ENOB = N - \log_2\left(\frac{\hat{\sigma}}{\sigma}\right) = \log_2\left(\frac{FSR}{rms\ noise \cdot \sqrt{12}}\right), \tag{13}$$

where N is the ENOB (resolution) of the ideal ADC, *rms noise* = $\hat{\sigma}$ is measured for actual converters with non-ideal transition function using formula ([1], Sect. 4.5.1.1):

$$rms\ noise = \hat{\sigma} = \frac{1}{M}\sum_{m=1}^{M}\left[V^{(m)} - \hat{V}^{(m)}\right]^2 \tag{14}$$

and $\sigma = \Delta^2/12$ is the *ideal rms quantization error* computed according to formula (3) where D and N_{ADC} should be replaced by the values FSR/2 and N, respectively. If DNL, INL, offsets, gain setting errors and other non-idealities of the analogue part are negligibly small, *rms noise* $\hat{\sigma} = \sigma = FSR \cdot 2^{-N}/\sqrt{12}$, and formula (13) becomes an identity $E = N$. Contrary to [1], where the value N is assumed to be given, for IC ADC this value is assessed according to (11).

Comparison of formulas (11) – (13) shows that definition of ENOB of IC ADC introduced in Sect. A generalizes the definition of the ideal ENOB N given in [1]. Assuming that *rms noise* of actual IC ADC is measured in the same way as *rms noise* of the flash ADC, that is according to (13), one may rewrite (11) in the equivalent form:

$$N_k = \log_2\left(\frac{\sigma_0}{\hat{\sigma}_k}\right) + \log_2\left(\frac{\hat{\sigma}_k}{\sigma_k}\right) = \hat{N}_k + \log_2\left(\frac{\hat{\sigma}_k}{\sigma_k}\right). \quad (15)$$

Values

$$\hat{N}_k = \log_2\left(\frac{\sigma_0}{\hat{\sigma}_k}\right) = N_k - \log_2\left(\frac{\hat{\sigma}_k}{\sigma_k}\right) = \log_2\left(\frac{FSR}{2\alpha\hat{\sigma}_k}\right), \quad (16)$$

in this formula represent the ENOB of actual IC ADC in full concordance with the definition given in [1] (see Eq. (13)). The single but principal difference concerns the definition of ENOB N_k of an ideal IC ADC where $\Delta_k = \sigma_k\sqrt{12}$ should be replaced by the assessment $\Delta_k = 2\alpha\sqrt{P_k}$, due to fast normalization of quantisation errors. Additional researches show that a similar correction is to be introduced also in definitions of ENOB of other classes of CADC and pipe-line ADC, which is to be measured according to (16), not (13).

In practice, the width of an ideal quantization interval $\Delta_k = 2\alpha\sqrt{P_k}$ can be assessed using simulations and measurement of the width of histograms of output quantization noise. For the greater numbers of cycles and Gaussian quantisation errors, Δ_k can be assessed using (14) and formula $\Delta_k = 2\alpha\sigma_k$. To assess the final ENOB of ideal IC ADC at the threshold point $n = n^*$, it is enough to assess Δ_n using histograms of the noise ν_k (or signal e_k) at the input of amplifier (A).

It is worth noting that in the threshold mode ($n = n^*$) of conversion, substitution of (12) into (9) and application of (7) and formula $n^* = F_0/2F$ (see Sect. 2.1.) permit to obtain the relationship:

$$R = 2FN^*\frac{F_0}{2}\log\left(1+\frac{W_{sign}}{W_{noise}}\right)\left[\frac{bit}{s}\right]. \quad (17)$$

Formula (17) is the analog of Shannon's formula [15] for channel capacity and determines the maximal information flow R through the converter, achievable under probability of appearance of rough errors (IC ADC overloading) not greater than a given small μ [9, 10, 12].

4. DIRECT MEASUREMENT OF ENOB

Computing the estimates $\hat{V}_k$ in the form of long binary words permits to *directly* measure the number of significant bits (denoted further as NOB_k, $k = 1, \ldots, n$) that is the number of "true" bits before the first erroneous bit (FEB) in the code $\hat{V}_k$. It is easy to see that NOB_k is equal to the number of zeros: $n_k^{(0)}(V)$ before the first unity (FEB) in the binary presentation of the conversion error $err_k^{bit} = \mathrm{mod}_2 |V - \hat{V}_k|$. To determine this number, it is sufficient to register the number of position $n_k^{(1)}(V)$ where the first unity in the binary word err_k^{bit} appears (in Fig. 4, FEB is denoted by unity). Values $NOB_k(V) = n_k^{(0)}(V) = n_k^{(1)}(V) - 1$ measured in this way depend on the current values of the input signal, therefore correct analysis of the conversion quality requires the application of statistical tools and assessment of distribution of NOB_k or FEB values. The

latter can be done using modelling technique [16] and histograms of NOB_k [5-7], which can be obtained in simulation experiments.

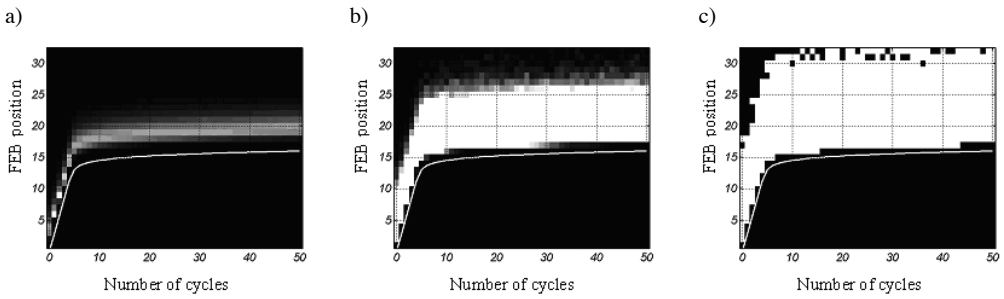

Fig. 7. Evolution of histograms of FEB positions (distinguished by white color) versus number of cycles: a) top-view; b) top view from the level of 50 hits; c) all the nonzero hits. White continuous line corresponds to ENOB measured indirectly.

A typical plot of changes of the histogram of FEB appearance in different positions of the output codes $\hat{V}_k$ depending on the number of cycles is presented in Fig. 7a. The brighter white color refers here to the higher frequencies of FEB appearance. In Figure 7b, the top-view of this histogram a from the level of 50 counts is shown, and in Fig. 7c all the non-zero FEB – counts in corresponding positions are shown. The plots permit to see a large amount of rarely appearing FEBs (Fig. 7c), and all FEBs that ever appeared in experiment (M = 10 000 samples). Continuous white lines in Fig. 7 a-c show the changes of ENOB computed using the basic definition (16) where *rms noise* $\hat{\sigma}_k$ was computed, for each $k = 1, \ldots, 50$, according to formula (14).

Analysis of histograms shows that the distribution of FEB has a sharp low boundary (see Figs 7c-d), which can be used as an assessment of the actual values of ENOB in sequential cycles of conversion. Preliminary investigations show that conventional indirect method of ENOB (16) measurement using *rms* (14) determines the low boundary of estimates of ENOB obtained in direct measurements. We must say that values of ENOB measured directly do not depend on any assumptions about dependencies of ENOB on ideal and real *rms noise*, as it is in indirect measurements, and give an objective information about the real resolution of the converters. The complex form of FEB (NOB_k) histograms shows the necessity of their careful statistical analysis and elaboration of measures and methods of IC ADC performance analysis and measurement most adequate and convenient for applications. This concerns also other classes of ADCs – it was established [6, 7] that FEB-histograms of each ADC have a complex asymmetric form, and heuristic definitions of ADC resolution and different methods of their measurement lead to different results.

5. CONCLUSIONS

The results of work show that most convenient for application and adequate characteristic of conversion quality is the effective number of bits (ENOB). It is shown that a perspective

way of improvement of the efficiency of cyclic ADC is the transition from low-bit logic to long binary word arithmetic in the code forming algorithm. This removes the limitations existing in conventional CADC and enables their optimization including the application of optimal data-processing algorithms and transition to a discrete scale of estimates [5-10, 12].

The transition considered in Sect. 3 from continuous to discrete scale of estimates (codes) permits to introduce, in a natural way, an analytical Eq. (12) for the ENOB, which can be directly connected with parameters of analogue elements and the code forming algorithm, parameters setting errors, non-linearities, statistic characteristics of the input signals and noise [5-10, 12]. There is shown the conceptual equivalence of the basic definition of ENOB so determined and given in [1]. However, for cyclic ADC this measure should be corrected, taking into account fast normalization of the conversion errors for the greater number of cycles (see formulas (12), (14), (16)).

The direct method of ENOB measurement discussed in Sect. 4, based on FEB-histograms permits not only to unify and make the assessments of CADC resolution more adequate and accurate, but also to elaborate more adequate and convenient testing methods for other classes of ADC. The complex structure of FEB-histograms shows the necessity to solve this task using advanced tools of statistical analysis and estimation theory.

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