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PERFORMANCE ASSESSMENT OF "FIELD PROGRAMMABLE ANALOG ARRAYS"

Field Programmable Analog Arrays (FPAAs) are reconfigurable analog modules introduced on the electronic market in the last decade. Their operation and, in particular, their programmability is achieved owing to the use of switched capacitors technology. At least in principle, they seem to be a very attractive and powerful tool to design analog circuits whose parameters have to be tuned to signal variations as in carrying out sensor conditioning systems. But the aim of exploiting their possibilities in the field of metrology requires complete characterization and performance assessment of the involved building blocks.

With this goal, in the paper, the metrological characterization of the most commonly blocks to be used in analog conditioning circuits, such as amplifiers and filters, is performed. These blocks have been characterized in terms of both frequency response and step response and the obtained experimental results have been compared with those expected from theoretic analysis. Concluding remarks are then deduced to furnish practical hints in the use of FPAAs in measurement applications.

Keywords: Measurements, analog filters, field programmable analog array, amplifiers

1. INTRODUCTION

Despite the fact that a large part of electronic circuitry now consists of digital logic, in several systems analog parts have still critical importance. As an example, in most cases, they are used to condition analog signals coming from sensors and actuators so that they can successfully be converted into digital form by analog-to-digital converters. Moreover, in some applications, even though powerful digital signal processors could perform the desired functions, it turns to be more convenient to exploit the same functionality, at a fraction of the application cost, with analog solutions. In conclusion, it is always a good design strategy to tailor the final application as the result of a correct balance between analog and digital load.

By the end of the last decade a new type of analog circuit, based on configurable blocks, the Field Programmable Analog Array (FPAA) has been introduced on the

market. The FPAA is a single chip, based upon switched capacitor circuit technology, that can be easily configured and dynamically reconfigured in order to implement a variety of analog functions, called Configurable Analog Modules (CAMs) (e.g. summing, amplification, differentiation, integration, filtering and so on) [1].

Analog resources are contained in multiple identical Configurable Analog Blocks (CAB) which incorporate operational amplifiers, capacitor arrays, CMOS switches and Static Memories (SRAMs) [2]. Analog functions such as programmable gain stages, adders, rectifiers, sample and hold circuits, and first order filters can be implemented in a single CAB [3]. Higher level functions, such as biquadratic filters, level detectors, and so on, can be implemented using two or more cells [4].

The most relevant FPAA feature is certainly provided by the opportunity to dynamically reconfigure the analog blocks. This feature, in fact, can be properly used to tune the characteristics of the analog section to the design requirement. This feature is particularly attractive in sensor conditioning applications, where the possibility to dynamically tune and adapt the signal characteristics to the front end specifications, immediately turns out in the improvement of the sensor performance [5]. Moreover, in contrast with architectures built with dissipative components (i.e. resistors), the switched-capacitor technology used in FPAA implies very low power dissipation and, consequently, it requires smaller dimensions for a pre-fixed circuit complexity. In a previous work, the authors have already exploited the reconfigurability of FPAA technology for the realization of an adaptive conditioning section of an ultrasonic distance sensor [6]. In particular, the conditioning block consisted of a band-pass filter and an amplifier whose quality factor and gain were tuned to obtain the best metrological performance. As expected, the distance sensor performance is strongly dependent on the concurrence between the desired and actual quality factor and gain.

In fact, each technology is characterized by specific problems that can be observed in bandwidth limitation, in non-linear behavior, in parameter accuracy limitation, and so on. Hence, also FPAA technology is expected to suffer from some unwanted characteristics. For instance, capacitors in FPAA can assume only integer values, so some effects connected with quantization errors are expected to be observed. In conclusion, the FPAA output will be somewhat different from the expected one [7]. Thus, before being fascinated by FPAAs possibilities and before deciding to use them in measurement applications, an accurate metrological characterization of the implemented blocks is required in order to work at the correct evaluation of the involved uncertainty. In this paper, in particular, the CAMs exploited by the aforementioned distance sensor (inverting amplifier and band-pass filter) have been taken into account.

The authors have focused their attention on a specific device, the AN221E04, a component of the second generation family of FPAAs by Anadigm Company, whose architecture is shown in Fig. 1 [8]. It is a switched capacitor FPAA comprising a 2x2 matrix with four CABs, four configurable I/O cells and two dedicated output cells.

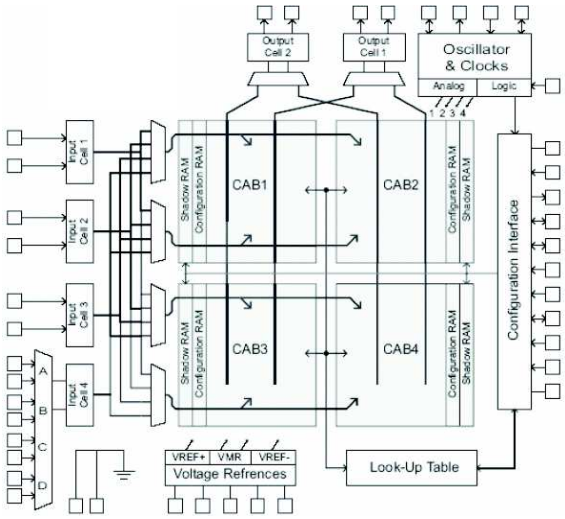

Fig. 1. Architectural scheme of AN221E04.

2. SWITCHED CAPACITOR TECHNIQUE

The Switched Capacitor (SC) technique is based on the consideration that a capacitor switched periodically between two circuit nodes is equivalent to a resistor connecting these nodes if the average value of current (over a period of time exceeding a number of times the switching period) is considered [9].

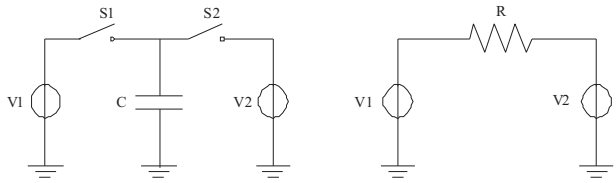

Fig. 2. SC circuit equivalent to a resistance.

A circuit diagram for this basic SC circuit is shown in Fig. 2. During the time when the switch S1 is closed and S2 is opened, the capacitor C is charged to the voltage applied to the input, V1. So the total charge on the capacitor C, in steady state conditions, is: $Q_1 = CV_1$.

When the switch position changes, i.e. S1 is opened and S2 is closed, C is charged or discharged depending on the applied voltage V2; however, in steady state, the total charge on the capacitor is: $Q_2 = CV_2$.

The net charge transferred from the input to the output during one switching period is then:

$$\Delta Q = Q_1 - Q_2 = C\,(V_1 - V_2)\,. \tag{1}$$

The mean value of the current flowing from the input to the output is:

$$I = \frac{\Delta Q}{T} = \frac{C\,(V_1 - V_2)}{T}. \tag{2}$$

This is equivalent to a current I flowing in a resistor whose value can be easily calculated:

$$I = \frac{V_1 - V_2}{R} \Rightarrow R = \frac{T}{C}. \tag{3}$$

By properly modifying the switching period T and the capacitance value C, a wide range of resistances can be obtained. Hence, by adopting switched capacitors, it is possible to integrate a circuit behaving as a resistance, but with higher accuracy, lower power consumption and, so, in reduced silicon dimensions [10].

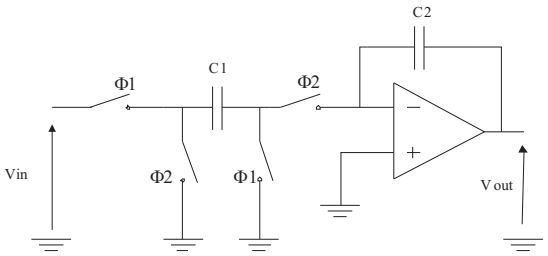

Fig. 3. SC circuit equivalent to an integrator.

Combining the scheme in Fig. 2, with op amps, various analog functions can be achieved. As an example, in Fig. 3 an integrator circuit, realized through switched capacitors is shown. Φ1 and Φ2 represent the phases during which a group of switches is closed, according to the clock scheme depicted in Fig. 4; T is the circuit clock, called master clock [11].

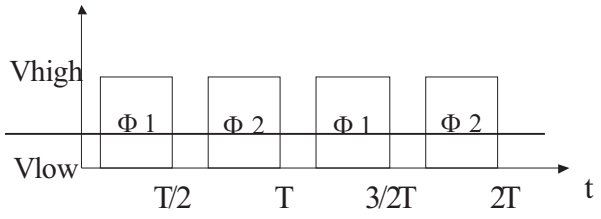

Fig. 4. Switching clock scheme for an integrator.

3. ASSESSMENT OF CAM PERFORMANCE

The AN221E04 by Anadigm is composed of four CABs, each one comprising eight banks of equally-sized capacitors that can assume a relative value between 0 and 255 units of capacitance.

The values of the programmable components of the CAB cannot be changed directly by the user, since the programming and constructive details are left unknown be Anadigm. In order to configure the desired circuit into the FPAA, the Anadigm Designer 2 software has to be used, along with a set of pre-built modules [12]. The user can link these modules and set parameters like amplifier gain, filter central frequency, integration constants and thresholds of comparators. As an example, in Fig. 5, a lowpass filter and amplifier have been programmed. Once the circuit has been designed, Anadigm software programs and configures the FPAA device as requested. At this aim, the microcontroller (PIC 16F876 by Microchip) manages byte transmission, through an asynchronous serial communication protocol.

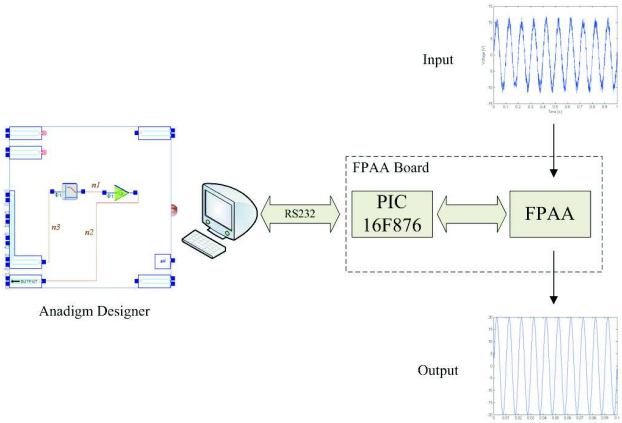

Fig. 5. Scheme of FPAA configuration.

Moreover, the Anadigm software provides a set of C functions to be used for reconfiguring the chip *on the fly* if design parameters require to be dynamically changed.

In the following, two types of CAM, widely used in electronic circuits and, in particular, in sensor conditioning applications, are considered for their behavior assessment: amplifiers and filters [8, 13].

The realized measurement station for experimental tests consists of a development board including the FPAA under test AN221E04; an Agilent 33220A signal generator (14 bit resolution, 20MHz maximum generation frequency, 20V peak-to-peak maximum voltage); a Tektronix TDS 210 digital oscilloscope (8 bits resolution, 60 MHz bandwidth, 1GS/s maximum sample rate). A personal computer is controlling the instruments to manage the measurement process (by means of a software developed in

LabVIEWTM environment and the IEEE-488 communication standard), and the FPAA for dynamic reconfiguration (through Anadigm Designer and RS232 communication standard).
The ideal transfer function of the amplifier is:

$$\frac{V_{out}(s)}{V_{in}(s)} = G. \tag{4}$$

The SC circuit realizing this CAM is shown in Fig. 6. The capacitor values are chosen based on the best ratios of the capacitors satisfying the following relations:

$$G = \frac{C_{in}}{C_{out}}. \tag{5}$$

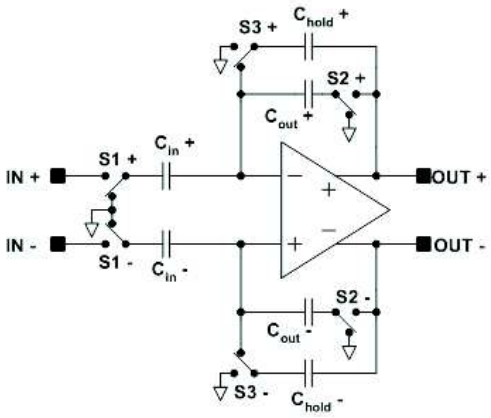

Fig. 6. SC circuit to realize an amplifier.

Obviously errors due to finite bandwidth, finite input impedance and finite gain of op amps and quantization cannot be neglected. With the aim of investigating the actual characteristics in comparison with theory, several parameters have been investigated. Experimental results obtained about the amplifier frequency response are reported in Fig. 7. The input was a sine wave with logarithmic frequency sweep in the range from 100 Hz to 15MHz. Actual gain and phase delay of the output are plotted versus frequency for different values of the nominal gain.

The experience put in evidence that the frequency response is quite flat inside the 100 kHz bandwidth declared by Anadigm. Furthermore, the flatness remains unaffected by the value of the settled gain. The amplifier phase delay is practically negligible up to 20 kHz, independently from the settled gain and then increases rapidly with frequency and gain. As for the gain value, significant difference between the nominal set gain and the measured one has been experienced; in particular, the higher the desired gain, the greater the obtained difference. The discrepancies seem not to depend on the

capacitances accuracy but they are mainly due to the saturation of the output amplifier. In fact, the same discrepancies have been observed by fixing the gain and by varying the input amplitude to observe the same output voltage. Results obtained for Integral Non-Linearity (INL), evaluated as the difference between the output voltages and the voltages associated with the interpolated transfer function, are shown in Fig. 8.

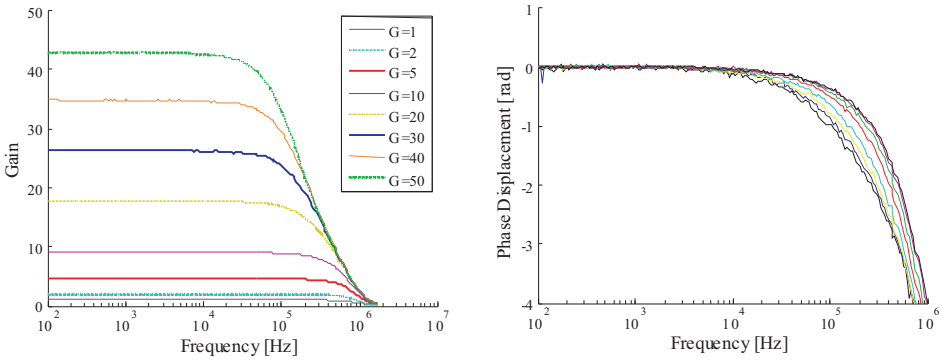

Fig. 7. Amplifier frequency response.

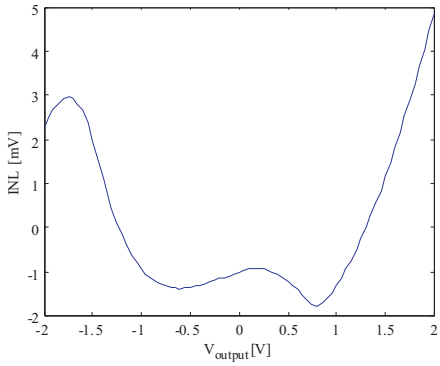

Fig. 8. Amplifier Integral Non-Linearity.

INL is lower than −2mV when the voltage output is within the range ±1V, whereas it rises up to 5mV when the voltage output swing increases to ±2V.

Both INL and gain error behaviors suggest that in order to remain inside a 1% gain accuracy, the output span does not have to exceed $\pm 1V_{PEAK}$.

The amplifier step response to a 20mV input step is presented in Fig. 9. Though, in theory, this should be a zero-order system, the device output evidences a slight overshoot in low gain configurations. In Table 1, the most significant parameters measured

at the output of the device supplied with the 20 mV step are reported versus gain variations. In particular, the response time and settling time arise along with the gain, whereas the slew rate decreases.

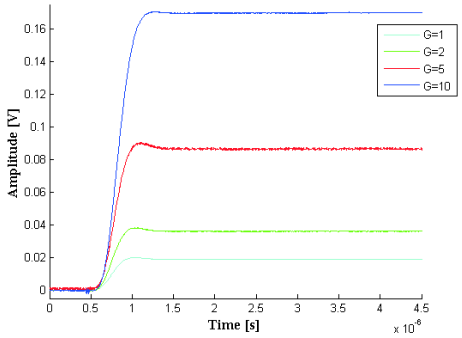

Fig. 9. Amplifier step response.

Table 1. Step response parameters of the amplifier.

Gain	Slew Rate (V/μs)	Response Time (μs)	Settling Time (μs)	Overshoot
1	3.3109	0.429	0.832	0.0579
2	3.2148	0.437	0.833	0.0623
5	2.9420	0.474	0.905	0.0431
10	2.3738	0.572	0.706	0.0037
20	1.4241	0.816	1.540	0.0030
30	0.9965	1.088	1.962	0.0015
40	0.7231	1.432	2.907	0.0006
50	0.6337	1.701	3.458	0.0001

A similar analysis has been performed on analog filters. As an example, the results obtained in experimental tests conducted on a biquadratic bandpass filter are given in the following. Figure 10 shows the switched capacitor (SC) circuit implemented in the device under test to realize a second order bandpass filter.
The ideal transfer function is:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-2\pi f_0 \frac{G}{Q} s}{s^2 + \frac{2\pi f_0}{Q} s + 4\pi^2 f_0^2}. \tag{6}$$

Capacitor size is chosen according to the following equations:

$$f_0 \cong \frac{f_c}{2\pi} \sqrt{\frac{C_2 C_3}{C_A C_B}}, \tag{7}$$

$$G \cong \frac{C_p}{C_4}, \tag{8}$$

$$Q \cong \frac{1}{C_4}\sqrt{\frac{C_2 C_A C_B}{C_3}}. \tag{9}$$

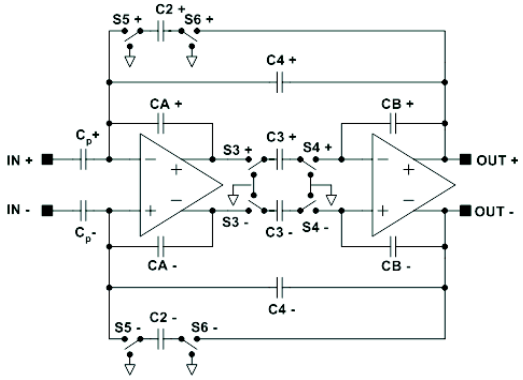

Fig. 10. SC circuit operating as a bandpass filter.

As aforementioned, the user selection of the central frequency, gain and quality factor of the filter are achieved by properly varying the capacitance values as stated from Eqs. (7), (8), and (9).

Filter performance in the frequency domain has been assessed by evaluating its frequency response in the presence of three different values of gain (1, 5, and 10), quality factor (5, 10, and 15) and central frequency (1 kHz, 50 kHz, and 400 kHz). For each experimental configuration, actual gain, upper and lower passband frequencies, upper and lower stopband frequency and quality factor have been evaluated. The obtained results have been compared with the characteristics obtained by means of two models developed in Matlab® software through the ideal transfer function given in (6) with (*i*) the desired parameters and (*ii*) the "quantized" parameters approximating that desired, but obtained from Eqs. (7), (8) and (9). By comparing results of the two models implemented according to the ideal transfer function, the quantization error has been estimated as

$$\Delta G_q = G_{quantized} - G_{theoretical}, \tag{10}$$

where $G_{theoretical}$ is the gain simulated by the Matlab transfer function with desired parameters, whereas $G_{quantized}$ is simulated by the transfer function with quantized parameters.

By comparing the characteristics obtained by the quantized parameter transfer function with those measured on the actual circuit, the gain tolerance has been evaluated as:

$$\Delta G = G_{actual} - G_{quantized}, \tag{11}$$

where G_{actual} is the actual gain measured at the output of the device under test.

As an example, Fig. 11 plots the filter output along with the Matlab theoretical and quantized responses corresponding to (*i*) central frequency of 1 kHz, (*ii*) unity gain and (*iii*) quality factors of 5, 10, 15.
At the bottom of the same figure, the errors expressed by Eqs. (10) and (11) are reported.

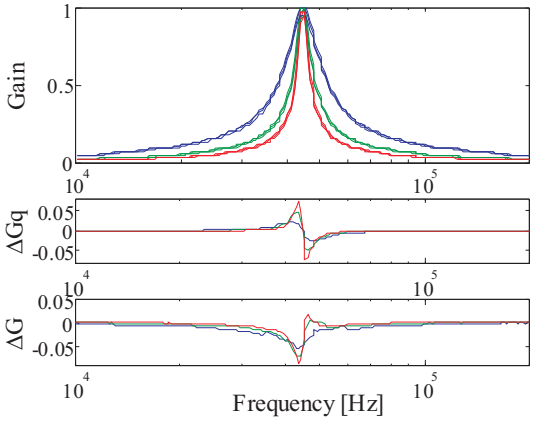

Fig. 11. Comparison between filter responses with ideal parameters, quantized parameters, actual parameters.

As shown in the figure, both errors ΔGq and ΔG are negligible within the considered frequency range, except for the frequencies close to the desired filter central frequency where the worst error is experienced. This behavior of the gain error reveals that the actual filter is centered on a frequency slightly different from that selected one: the higher the selected quality factor, the greater the errors.

In order to reach a better understanding of the phenomena, the central frequency has been changed from 1 up to 100 kHz. It has been observed that the filter response shows a shape similar to Fig. 11. By measuring the actual central frequency, the experiments confirmed the aforementioned hypothesis; in fact, an error affecting the filter resonance frequency contained within 1% of the expected value has been observed. In Table 2, as an example, results obtained for a 40kHz nominal frequency are reported. In particular, the differences between the nominal central frequency and the frequency associated with maximum gain, for different quality factors, have been considered.

Table 2. Filter frequency error for f_{nom} = 40 kHz.

Q	$f_{max\,G}$ [kHz]	$f_{max\,G} - f_{nom}$ [kHz]	$f_{max\,G} - f_{nom}/f^{*}_{nom}100$
0.707	39.90	−0.10	0.25%
1.42	39.80	−0.20	0.50%
5.65	39.80	−0.20	0.50%
14.1	39.78	−0.22	0.55%
70.7	39.76	−0.24	0.60%
99.7	39.71	−0.29	0.72%

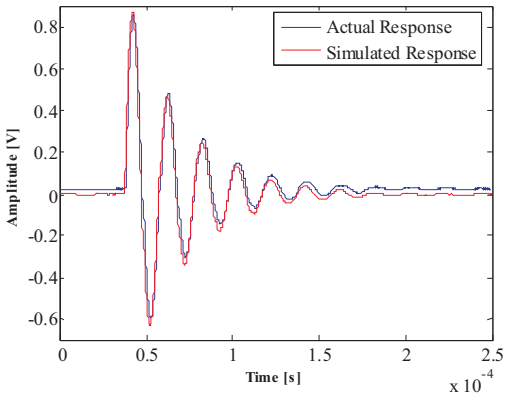

Fig. 12. Filter step response.

Filter behavior in the time domain has also been investigated by means of its step response. In Figure 12 the step response of the simulated model and the step response obtained by experimental tests are matched. Clearly, apart from an offset experienced in the actual response, the filter real step response agrees very well with the ideal response. The offset could represent a problem when the bandpass filter would belong to a conditioning chain including other blocks operating on signal amplitude, such as amplifiers. This drawback can, in fact, result in a saturated output of the FPAA with loss of information of the input signal.

Other time domain parameters have been measured and are reported in Table 3.

Table 3. Step response parameter of the filter.

Gain	Damping Time Constant (μs)	Ringing Frequency (Hz)
5	36	50000
QF	Settling Time (μs)	Overshoot (V)
5	139	0.85

As expected, the step response behaves as a second order narrow bandwidth system. The time constant and, consequently, settling time are, in fact, rather high. Moreover, the ringing frequency has been found equal to the natural frequency of the filter, i.e. its center frequency.

4. CONCLUDING REMARKS

The paper deals with the Field Programmable Analog Array, a recent device that has shown to be very useful whenever the characteristics of analog conditioning blocks have to be changed *on-the-fly*. In particular, the performance of one of the most adopted FPAA, i.e. AN221E04 by Anadigm, has been assessed. Principal blocks, such as amplifiers and filters, have been considered.

As far as it concerns the amplifier, the following conclusions can be summarized: in the gain range $1 \div 50$, the discrepancy between the actual in-band gain and the designed one has been measured and never exceeds ± 0.5 dB. The observed discrepancy is expected to depend mainly on the saturation effect of the output amplifier. In particular, we suggest to maintain the output swing inside ± 1 V in order to obtain an accuracy of 1%. The effect of the quantization error introduced by the programmable capacitances that can assume only quantized values ($0 \div 255$ capacitance units) is, instead, negligible. Good results have been experienced also in the amplifier frequency response, where the actual -3 dB bandwidth reproduces with high fidelity the $0 \div 100$ kHz range declared by Anadigm. Also satisfactory is the response in terms of in-band ripple.

As for the filter characterization, different tests have been carried out in order to verify how faithfully the filter response matches the one expected by its mathematical model. In particular, parameters such as gain, passband and stopband frequencies have been taken into account. The achieved results show a slight difference between the amplification nominal set value and the measured one. Also in this case the output swing is a limiting factor.

In conclusion, even though some discrepancies between the design parameters and actual measurements have been evidenced, FPAA devices are of sure interest in the realization of conditioning systems where flexibility is a major constraint compared with parameter accuracy.

Instead, in applications in which parameter accuracy should represent a major constraint, the device can no more be used so as it is (i.e. being confident in the specifications deduced from the implemented theoretical models). However, the authors are working to increase parameter accuracy with proper closed loop strategies, able to exploit device flexibility to compensate *on-the-fly* block parameters, thus gaining the accuracy requested by more constraining applications.

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